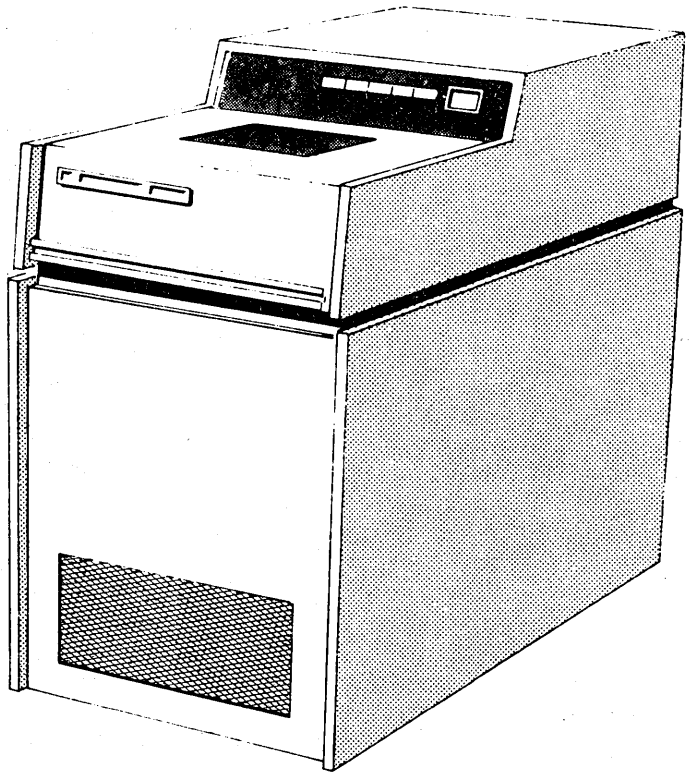
CONTROL DATA
CORPORATION

CONTROL DATA®
BR3D4 DISK STORAGE UNIT



REFERENCE MANUAL

REVISION RECORD

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or use Comment Sheet in the back of this manual.

PREFACE

This manual has been prepared for customer engineers and other technical personnel directly involved with maintaining the Disk Storage Unit (drive).

Reference information is provided in six sections in this manual. Section numbers and a brief description of their contents are listed below.

Section 1 - General Description. Describes equipment functions, specifications, and equipment number identification

Section 2 - Operation. Describes and illustrates the location and use of all controls and indicators, power on sequencing, and disk pack installation and removal.

Section 3 - Theory of Operation. Describes basic logic and mechanical functions.

Section 4 - Introduction to logic symbology and card constructions.

Section 5 - Description of integrated circuits used in the drive. Includes pin assignments along with truth tables and/or typical waveforms.

Section 6 - Description of discrete components and their functions. For ease of using the logic diagrams, transistors and their associated components are frequently condensed into an equivalent logic symbol. This section, arranged in alphabetical order of the circuit type designator (AAA-ZZZ), explains these functions and illustrates the actual discrete elements.

Manuals applicable to the BR3D4 Disk Storage Units are as follows:

Publication No.	Title
83313100	Maintenance Manual
83313200	Reference Manual
83313300	Parts Data

CONTENTS

FIGURES

TABLES

SECTION 1

GENERAL DESCRIPTION

INTRODUCTION

The CONTROL DATA® BR3D4 Disk Storage Unit is a high speed, random access, disk storage device. Data is recorded on removable disk packs. Equipment specifications are listed in Table 1-1.

ASSEMBLY LOCATIONS

Figure 1-1 illustrates the major drive assemblies. Detailed information on the construction and function of these assemblies is provided in Section 3 of this manual.

TABLE 1-1. DRIVE SPECIFICATIONS

Characteristics	Conditions	Specifications
PHYSICAL SPECIFICATIONS		
Size	Height	39.5 in. (100 cm)
	Width	22 in. (56 cm)
	Depth	44.5 in. (176 cm)
Weight		660 lbs (300 kg)
Temperature	Operating	60°F (15.5°C) to 90°F (32°C)
	Gradient	12°F (6.6°C) per hour
	Non-Operating	-30°F (-34°C) to +150°F (66°C)
Relative Humidity (no condensation)	Operating	20% to 80%
	Non-Operating	5% to 95%
Altitude	Operating	-1000 ft (-305 m) to +10,000 ft (3.05 km) mean sea level
	Non-Operating	-1000 ft to +35,000 ft (10.7 km)
POWER SPECIFICATIONS (Typical Values)		
Refer to Installation Manual for additional power information. Definitions: Standby State: dc power on, spindle motor off. Accessing State: positioner continually random seeking.		
AC Power Input	BR3D4A	208v (±10%), 60 (±0.6) Hz, 3-phase
	BR3D4B	220v (±10%), 50 (±0.5) Hz, 3-phase
	Phasing (60 Hz)	Two phases supplied from a three-phase Wye source are used per 60 Hz drive. Three-phase power is available at A1TB1 by power cable. During installation, two phases are connected to internal power supply. Phases are normally rotated from drive-to-drive so that each group of three drives present a balanced three-phase load. Motors are single-phase connected phase-to-phase.
	Phasing (50 Hz)	One phase is used per 50 Hz drive. Three-phase power available at A1TB1 by power cable. Power is connected phase-to-neutral with phases rotated from drive-to-drive to present a balanced three-phase load.

TABLE 1-1. DRIVE SPECIFICATIONS (CONT'D)

Characteristics	Conditions	Specifications
Current (208v at 60 Hz)	Standby	2 amp/phase
	Starting	34 amp/phase for 7 seconds
	Accessing	8 amp/phase
Power True (208v at 60 Hz)	Standby	0.4 kilowatt
	Accessing	1.2 kilowatt
Power Factor (208v at 60 Hz)	Standby	0.9
	Accessing	0.7
Heat Dissipation (208v at 60 Hz)	Standby	1400 BTU/hr (353 Kg-cal/hr)
	Accessing	4200 BTU/hr (1060 Kg-cal/hr)
DATA RECORDING SPECIFICATIONS		
Disk Pack	Packs/Drive	1
	Recording Surfaces/ Disk Pack	19
	Usable Tracks/ Recording Surface	823 (808 plus 15 spares)
	Tracks/Cylinder	19
	Tracks/Inch	384
	Tracks Spacing	0.0026 inch (nominal)
	Rotational Speed	3600 (±2%) rpm (16.7 ms/rev)
	Recommended Pack	CDC 9883-61
Seek Timing	Access Mechanism	Voice Coil driven by servo loop
	823 Tracks	55 ms (maximum)
	1 Track	10 ms (maximum)
	Average	30 ms
Latency Time	Average	8.33 ms (@3600 rpm)
	Maximum	17 ms (@3528 rpm)
Recording	Mode	Modified Frequency Modulation (MFM)
	Bit Density	4040 bpi (inner track nominal)
	Rate	6.45 MHz (nominal)
Heads	Quantity	19 recording
		1 servo (positioning)
	Read/Write Width	0.0021 in. (nominal)
Controller/Drive	Quantity	2 per channel
Interface Cables	Maximum Length	50 ft (15m)
	Connectors	4 per drive
	Pin Assignments	Refer to Installation Manual
	Signal Functions	Refer to Section 3 of this manual

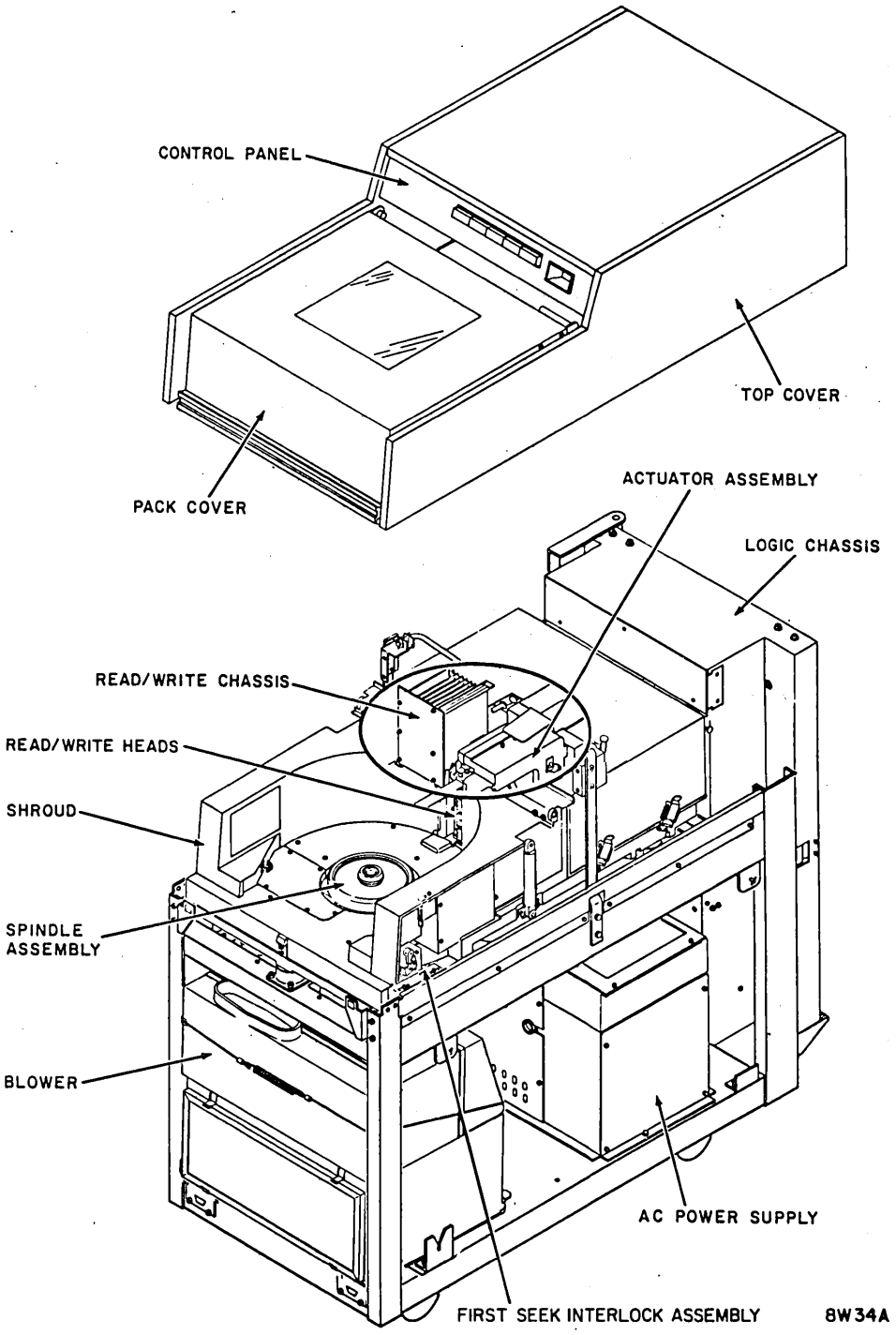


Figure 1-1. Assembly Locations

TOP COVER ASSEMBLY

The top cover assembly protects the drive assemblies during customer operations.

The pack cover is opened by means of a latch under the cover. An electrical switch senses the cover is opened, and disables spindle motor power.

DECK ASSEMBLY

The deck assembly has the following major subassemblies:

- A spindle assembly to mount the disk pack. Its associated drive motor runs continuously whenever a pack is installed, the pack cover is closed, the START switch is on, and sequence power (either from the controller or with the LOCAL/REMOTE switch on the power supply in the LOCAL position) are available.
- An actuator assembly that mounts the read/write heads for processing data. The actuator contains a voice coil positioner controlled by a closed-loop, continuous-feedback servo system.
- A shroud to surround the disk pack. The shroud: protects the pack, aids in directing air from the blower to the pack; and prevents the operator from damaging the read/write heads with the pack.
- A read/write chassis to mount logic cards that contain logic directly affecting head selection and operation.
- A first seek interlock assembly to provide a heads load command delay.

AC POWER SUPPLY

The ac power supply provides ac power required by the drive. The ac voltages generated are distributed to the dc power supply located in the logic chassis assembly.

The line filter filters the ac power input to the power supply.

LOGIC CHASSIS

The logic chassis serves as the mounting point for the main complement of the logic cards and dc power supply. The chassis is hinge-mounted for easy access to the cards (which plug in at the inner side of the chassis) or to the backpanel terminals (at the outer side). The backpanel terminals provide ready access to all signals entering and leaving each card. In addition, the cards have test points for monitoring critical signals within the cards.

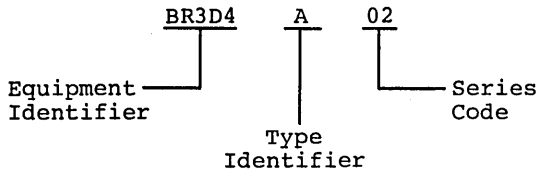
The logic chassis also contains a test point panel that provides a location for status monitoring of the dc voltages generated by the dc power panel.

Located in the lower half of the logic chassis is the dc power panel. The dc power panel provides dc power required by the drive. It also contains relays and solid state logic used for power sequencing.

EQUIPMENT IDENTIFICATION

An equipment number is assigned to each drive to identify its configuration. This provides a systematic method of identifying, accounting, and controlling changes that affect drive logic and mechanical components.

The equipment configuration is identified by a nameplate attached to the frame at the back of the drive. The nameplate is visible with the logic chassis open. The Equipment Identification Number will be similar to the following:



The Equipment Identifier indicates the basic function of the unit. This number will be BR3D4 on all units for which this series of manuals have been prepared.

The Type Identifier indicates a non-interchangeable difference in equipments that affects the interface. The term "Mod" is sometimes used interchangeably with "Type Identifier". The following identifiers have been assigned:

Engineering Number	Channel Configuration	Volts/ Frequency
BR3D4A	Single	208/60 Hz
BR3D4B	Single	220/50 Hz

The Series Code changes with each non-interchangeable change within the equipment. Drives with different series codes are fully interchangeable at the system level; however, not all of their electrical or mechanical components may be interchangeable. Series codes are changed by Engineering Change Order (ECO) only at the factory.

Other changes are accomplished by Field Change Order (FCO). These changes may be installed either at the factory or by field personnel. FCO changes are indicated by an entry on the FCO Log that accompanies each machine. It is important that this log be kept current by the person installing each FCO.

Unless otherwise specified, all theory, procedures, and diagrams in these manuals apply to all units. Exceptions are noted where applicable.

Manuals accompanying unit shipments from the manufacturer match the configuration of those units. Subsequent manual changes are controlled by the Revision Record sheet behind the title page of every manual. This sheet identifies the Series Code and FCO effectivity of manual changes. If maintenance will be performed using a manual other than the manual supplied with each drive, verify that the manual and drive configurations match.

SECTION 2

OPERATION

CONTROLS AND INDICATORS

The drive contains several panels and indicators. Figure 2-1 locates the panels and indicators on a cabinet. Table 2-1 describes the various panel controls and indicators.

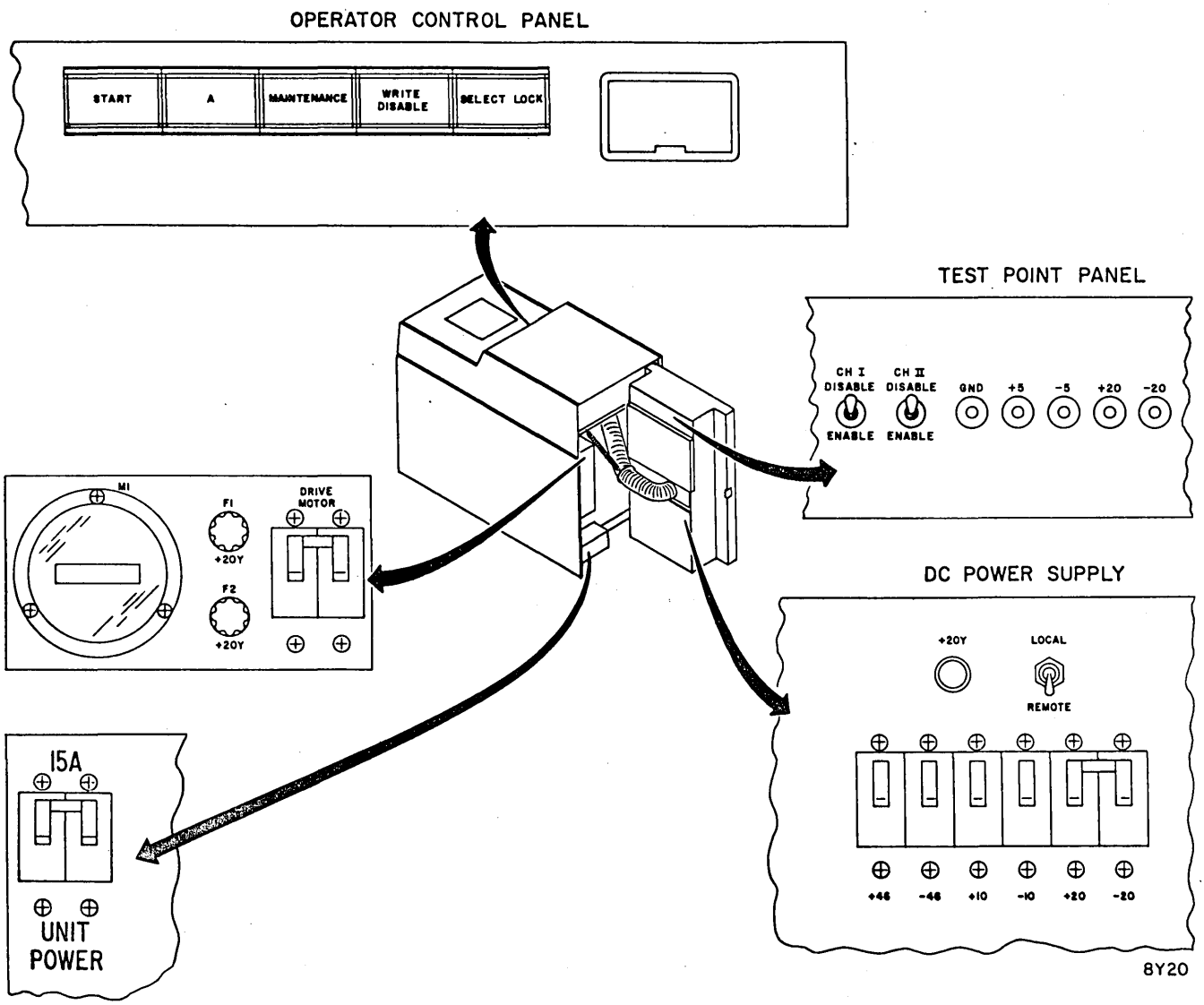


Figure 2-1. Controls and Indicators

TABLE 2-1. CONTROLS AND INDICATORS

Control or Indicator	Function
	OPERATOR PANEL
START switch/indicator	Switch energizes (when pressed to light) spindle drive motor and begins the First Seek sequence provided the following conditions are met: 1. Disk pack is in place and canister removed. 2. Pack cover is closed. 3. Circuit breakers are on. 4. Sequence power available either from control unit (if power supply panel LOCAL/REMOTE switch is set to REMOTE) or from power supply (if power supply LOCAL/REMOTE switch is set to LOCAL). Lights when switch is on and conditions 2 and 3 are met. This allows operator to know which units will sequence on when control unit sequence power becomes available. Switch causes a power off sequence when pressed while the indicator is lighted.
Physical Unit Identification indicator	The lens of this indicator may be either blank or lettered A through H to physically identify the unit. Indicator lights when read/write heads are loaded, a Logical Address Plug is installed and a Seek Incomplete status is not present. Half of indicator extinguishes when unit goes active.
MAINTENANCE indicator	Lights when related drive has experienced one of the following conditions: 1. Either ±10v circuit breakers on power supply panel set to OFF. 2. ON LINE/OFF LINE switch on CE Tester panel set to OFF LINE.
SELECT LOCK switch/ indicator	Lights when one or more of the following unwanted conditions occur: 1. Read and Write are selected at the same time. 2. More than one head is selected. 3. Voltage fault -Low voltage (±5v, ±20v, or -16v). If -16v is low, heads retract. 4. No servo tracks - Loss of servo track for 200 ms or more. Heads retract. 5. Write is selected without an On Cylinder signal. 6. Write gate is on but no write current (current fault). 7. Write gate is on during Index (write overrun). 8. Write current present without a Write Gate (current fault). 9. Write gate is on but no data transitions for 900 nsec (no write data or open coil). 10. Write gate is on with offset active.

TABLE 2-1. CONTROLS AND INDICATORS (CONT'D)

Control or Indicator	Function
WRITE DISABLE switch/ indicator	Switch inhibits (when pressed to light) write gate, preventing drive from writing on pack.
LOGIC ADDRESS PLUG (LAP) receptacle	A keyed LAP, when installed in this receptacle, assigns a logical address of 0 through 7 or Service to the drive.
	LOGIC CHASSIS TEST POINT PANEL
+5, -5, +20, -20, and GND test jacks	Provide a point at which dc voltages in logic chassis can be measured (do not use as a voltage source).
CH I DISABLE/ENABLE switch	Enables/disables channel I transmitters and receivers.
CH II DISABLE/ENABLE switch	Not used
	AC POWER SUPPLY
Elapsed Time Meter	Indicates cumulative hours that logic dc power is on.
DRIVE MOTOR circuit breaker	Controls application of ac voltage to spindle drive motor.
+20Y Fuses	Protects 20 volt power supply transformer used to derive +20Y sequence and lamp voltages.
	DC POWER SUPPLY
+20Y indicator	Lights to indicate presence of +20Y voltage used by lamps and power up sequence circuit.
LOCAL/REMOTE switch	Allows power up sequence to be controlled by either the control unit (when set to REMOTE) or by +20Y-vdc from power supply (when set to LOCAL).
±46, ±20, and ±10 volt circuit breakers	Control application of related dc voltages throughout drive.
	MAIN BREAKER BOX
UNIT POWER circuit breaker	Controls application of main ac power.

OPERATING INSTRUCTIONS

POWER APPLICATION

The following procedure prepares the drive to go on-line.

1. Install a disk pack (refer to Disk Pack Installation).
2. Set main breaker box UNIT POWER circuit to ON. Blower motor will begin to operate.
3. Open cabinet logic chassis gate and position DC power supply switches as follows:
   a. LOCAL/REMOTE switch to REMOTE. Power up sequence is then under system control. If maintenance is to be performed, set switch to LOCAL.
   b. Set all circuit breakers to ON.
4. The power supply +20Y indicator lights.
5. Close cabinet logic chassis gate.
6. Press operator panel START switch/indicator. The switch/indicator lights.
7. When control unit sequence power becomes available, or if in LOCAL mode, the First Seek operation begins.
8. The First Seek operation is complete when the heads are positioned at track 00. Operator panel Physical Unit indicator lights when the First Seek operation has been completed and a LAP has been installed. The unit is now ready to receive a command.
9. To stop spindle motor, press operator panel START switch. To remove power to drive, turn off UNIT POWER circuit breaker.

WARNING

If unit fails to power down when START switch is pressed, the following procedure must be followed to avoid personal injury.

   a. Open top cover from rear.
   b. Disconnect yellow lead from voice coil.
   c. Manually retract heads.
   d. Determine cause of failure (normally an open lead to voice coil).

DISK PACK HANDLING

To ensure maximum disk pack life and reliability, observe the following precautions:

1. Store disk packs in a machine-room atmosphere (60°F to 90°F, 10% to 80% relative humidity).
2. If a disk pack must be stored in a different environment, allow two hours for adjustment to the computer environment before use.
3. Never store a disk pack in sunlight, in a dirty environment, or on top of another disk pack.
4. Store the disk packs flat, not on edge.
5. Always be sure that both the top and bottom plastic covers are on a disk pack whenever it is not actually installed in a drive.
6. When marking packs, use a pen or felt-tip marker that does not produce a loose residue. Never use a led pencil. Write on the label before it is applied to the disk pack.

DISK PACK INSTALLATION

Make certain that the disk pack to be installed has been properly maintained.

1. Raise drive front cover.
2. Lift the disk pack by the plastic canister handle.
3. Disengage the bottom dust cover from the disk pack using the knob in the center of the cover. Set the cover aside to an uncontaminated storage area.

CAUTION

Make certain the heads are fully retracted.

4. Place the disk pack onto the spindle.

NOTE

A spindle lock mechanism (ratchet brake) is actuated when the disk pack canister cover is on the spindle. A "click" may be heard as the lock mechanism engages. The mechanism holds the spindle stationary while loading or unloading a disk pack.

5. Twist the canister handle clockwise until pack is locked in place.

6. Lift the canister clear of the disk pack and set it aside to an uncontaminated storage area.

7. Close the front cover immediately to prevent the entry of dust and the contamination of the disk surfaces.

DISK PACK REMOVAL

1. Press (to extinguish) the operator panel START switch.

2. Check that disk pack rotation has stopped completely.

3. Raise the front cover.

CAUTION

During maintenance procedures the read/write heads are sometimes manually positioned. Make certain that the heads are fully retracted.

4. Place the plastic canister over the mounted disk pack so that the post protruding from the center of the disk pack is received into the canister handle.

5. Twist the canister handle counterclockwise until the disk pack is free of the spindle.

CAUTION

Avoid abusive contact between the disk pack and the spindle assembly.

6. Lift the canister and the disk pack clear of the spindle.

7. Close the front cover.

8. Place the bottom dust cover in position on the disk pack and tighten it.

9. Store the disk pack in a clean cabinet or on a clean shelf.

SECTION 3

THEORY OF OPERATION

INTRODUCTION

Theory of operation for the drive is organized into two parts. The first part describes the major mechanical assemblies. The second part describes the logical functions and the signals exchanged with the controller.

Functional descriptions are frequently accompanied by simplified logic diagrams. These diagrams are useful both for instructional purposes and as an aid in troubleshooting. Figure 3-1 illustrates the logic symbology used by the illustrations in this manual. The diagrams have been simplified to illustrate the principles of operation; therfore, other elements may be omitted. The logic diagrams in the Maintenance manual should take precedence over the diagrams in this section whenever there is a conflict between the two types of diagrams.

The descriptions are limited to drive operations only. In addition, they explain typical operations and do not list variations or unusual conditions resulting from unique system hardware or software environments. Personnel using this manual should already be familiar with principles of operation of the computer system, the controller, programming considerations (including the correct sequencing of I/O commands and signals), and track format (i.e., data records and field organization).

ASSEMBLIES

Refer to Section 1 for major assembly locations.

POWER SUPPLY

Each drive cabinet has a self-contained power supply accessible by swinging open the logic chassis. The power supply is contained in two locations. The ac portion of the supply, consisting of transformers, rectifiers, triacs, and line filters, is mounted in the lower rear of the drive cabinet. The dc portion of the supply, consisting of rectifiers and filters and the relays for power sequencing, is mounted in the lower portion of the logic chassis. Power supply cooling is accomplished by room air for the ac portion; for the dc portion, cooling air is blown over the chassis from a blower at the front of the drive cabinet.

The power supply has the following onputs:

1. +20Y for power sequencing control.
2. ±20 vdc used by the logic.
3. ±9.7 vdc which, in turn, is regulated to ±5 vdc at the logic chassis.
4. ±46 vdc for use by the voice coil positioner.
5. -16 vdc used to retract the carriage under emergency conditions.

Power distribution and sequencing control are illustrated in Figures 3-2 through 3-4.

AC/DC Distribution

Input power is made available to the power supply via the closed contacts of the UNIT POWER circuit breaker. With this breaker closed, the blower motor operates. AC power is available to the remainder of the circuit breakers.

The remainder of the ac distribution occurs when the input voltage is applied to transformer A1T3. An ac voltage of about 24 volts is picked off the secondary and applied to the first seek interlock motor, but application of the voltage to the motor does not occur until the spindle motor is started. Another T3 output is rectified to +20Y volts, which is used as a control voltage within the power system.

With +20Y volts available, A1Q1 is enabled. Solid state switches A1Q1 through A1Q4 effectively operate as relays.

The input applied to pin 1 of these devices is transferred to output pin 2 only if pin 3 has +20 volts on it while pin 4 is grounded. These enables are described in detail in the Power Up Sequence discussion.

With A1Q1 enabled, ac is applied to transformers A1T1 and T2. In the case of T2, four distributative voltages developed across the secondary windings are applied to receifier/filter circuits. The four circuits (+9.7, -9.7, +20, and -20 vdc) are not adjustable and incorporate no switching device other than circuit breakers for circuit protection. Both polarities of the 9.7v circuit are voltage level regulated and made adjustable to ±5 vdc at the logic chassis.

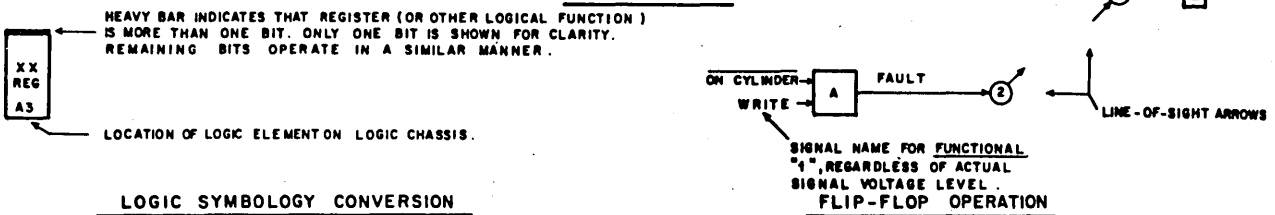
The voltages developed across A1T1 are applied to rectifier and filter circuits. None of the voltages are adjustable. The actuator power (±46 vdc) incorporates no switching devices other than circuit breakers for protection. The emergency retract power (-16 vdc) uses retract relay K5 to connect or disconnect the emergency retract capacitor to the voice coil. This function is explained further in the Emergency Retract discussion.

GENERAL INFORMATION

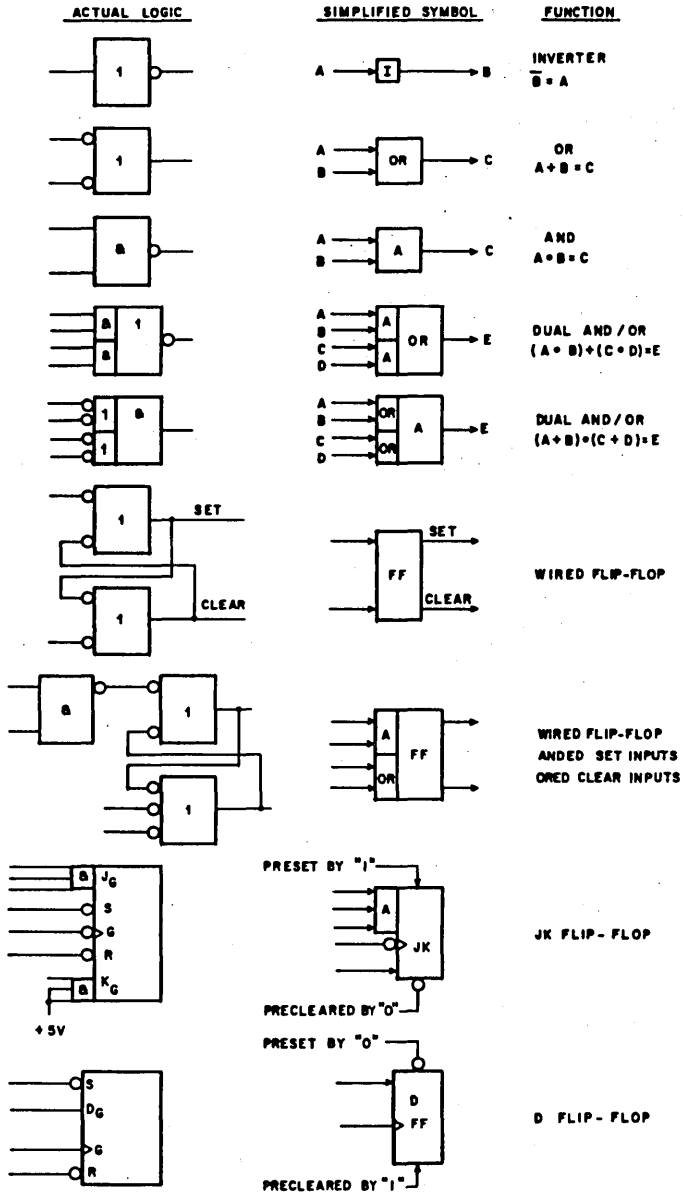
SIMPLIFIED DIAGRAMS IN THIS MANUAL SHOW THE FUNCTIONAL FLOW OF SIGNALS THROUGH THE DRIVE. THE DIAGRAMS HAVE BEEN SIMPLIFIED TO SERVE AS A GUIDE IN TROUBLESHOOTING AND IN UNDERSTANDING DRIVE OPERATIONS. REFER TO THE COMPLETE LOGIC DIAGRAMS FOR ACTUAL TEST POINTS AND SIGNAL LEVELS.

ALL LOGIC IS SHOWN ON POSITIVE LOGIC REPRESENTATION. SIGNAL LEVELS ARE DISREGARDED. ALL SIGNALS ARE NAMED WHEN THE FUNCTION TO BE ACCOMPLISHED REQUIRES A LOGICAL 1, REGARDLESS OF ACTUAL SIGNAL VOLTAGE LEVEL.

SYMBOLS



LOGIC SYMBOLOGY CONVERSION



FLIP-FLOP OPERATION

WIRED FF

FF OUTPUTS ARE COMPLEMENTARY UNLESS BOTH INPUTS RECEIVE SIMULTANEOUS ENABLES. IF SO, BOTH OUTPUTS ARE HIGH ("1").

JK FF

JK FF IS ENABLED (TO CHANGE STATE) BY DYNAMIC TOGGLE. IF CIRCLE IS SHOWN AT TOGGLE, CIRCUIT IS ENABLED BY NEGATIVE-GOING TOGGLE ("1"→"0"). PRESETS AND PRECLEARS DO NOT REQUIRE TOGGLE TO CHANGE STATE.

JK TRUTH TABLE

J	K	BEFORE TOGGLE		AFTER TOGGLE	
		SET	CLEAR	SET	CLEAR
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

D FF

SAME AS JK, EXCEPT THAT THERE IS NO DATA INPUT TO CLEAR SIDE. FF SETS ONLY IF D INPUT IS "1" WHEN TOGGLE GOES TO "1". IF D INPUT IS "0" AT TOGGLE, FF CLEARS.

7H7

Figure 3-1. Simplified Logic Symbology

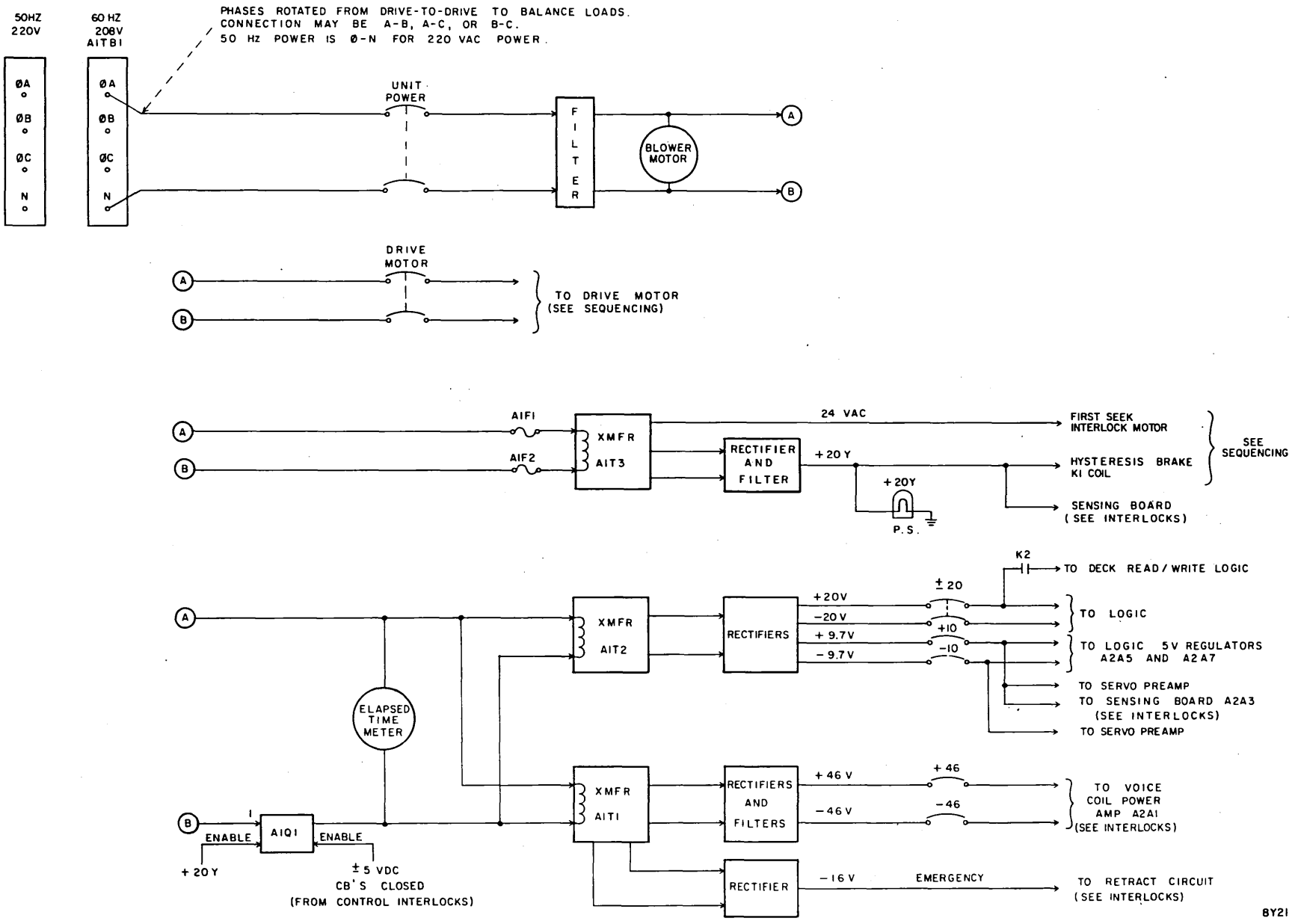


Figure 3-2. Power Distribution

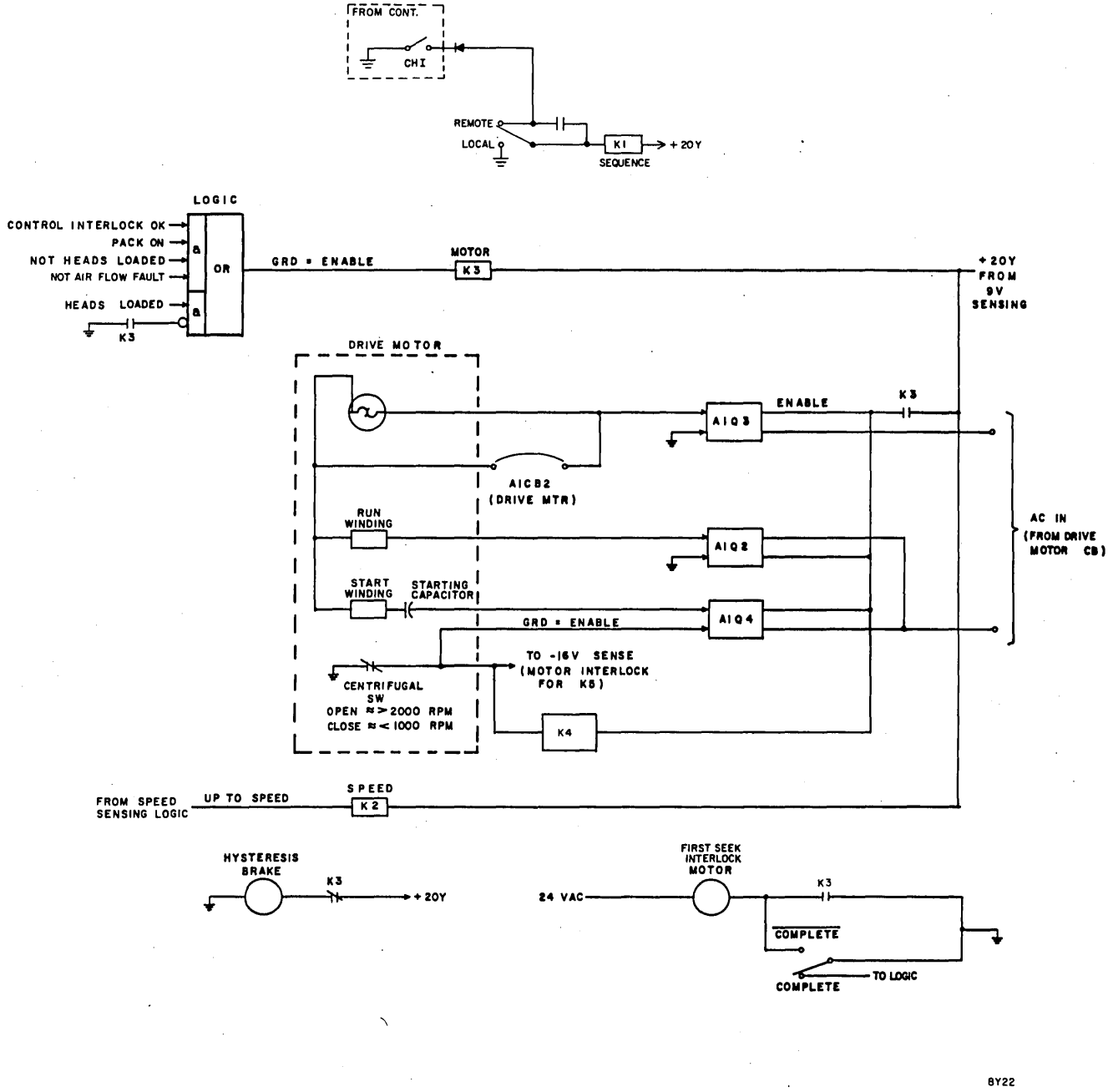


Figure 3-3. Power Sequencing

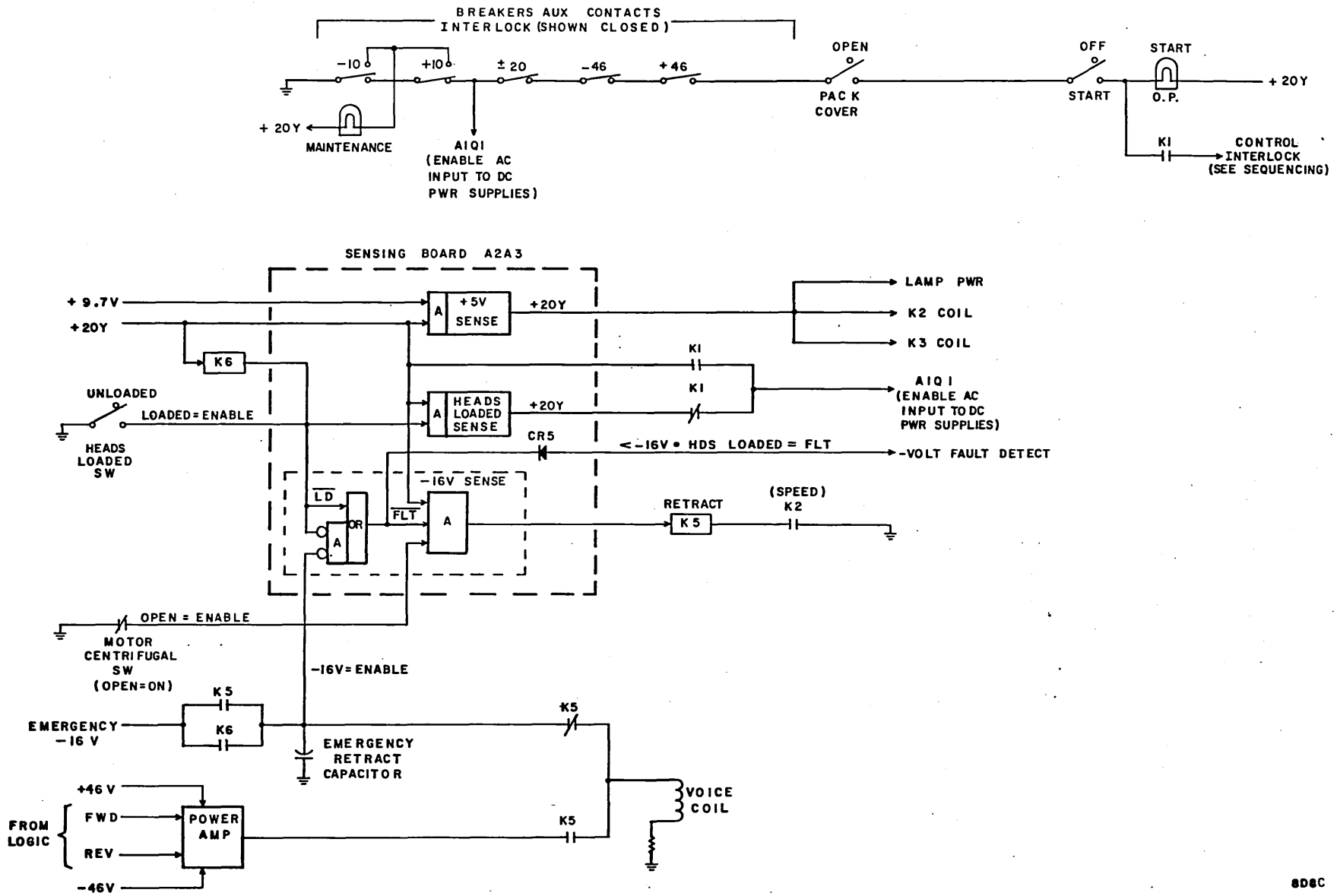


Figure 3-4. Power Interlocks

Overtemperature Monitoring

An air flow actuated switch is mounted in the DC power supply, at the bottom of the logic chassis. Loss of cooling air (excessive temperature) causes the switch to close. This has the following effect:

1. The SELECT LOCK indicator on the control panel lights.

2. Air Flow Fault (Bit 5) on Bus In is high if queried by Tag 12 BOB5 (Request Diagnostic Sense - Fault).

A high temperature condition prevents a power up sequence by inhibiting the energizing of K3 (Motor Start Relay). If the high temperature (loss of cooling air condition) is detected after power up and in a heads loaded condition, unit operation is not directly inhibited.

The logic temperature switch is kept open by normal air flow from the cooling blower. Low air flow allows the switch to close. A low air flow condition detected before heads are loaded, will de-energize Motor Relay K3.

Power On Sequence

Power application to a unit is sequenced by logic and by relays in the power supply. Refer to Figure 3-3. Assume that all circuit breakers are closed. If so, the blower motor is operating and the hysteresis brake is energized by +20Y.

Power on may be controlled either by the controller (remote) or locally for maintenance purposes (local). The Power On Sequence is as follows:

1. +20Y is connected to relay K1 either by placing the LOCAL/REMOTE switch in the LOCAL position or, in the REMOTE position, from the controller. (K1 contacts are in the switch circuit so that, once the unit is powered up, the LOCAL/REMOTE switch can be switched without dropping power, assuming ground is available from the controller.) Other contacts of K1 enable solid state switch A1Q1 to turn on the elapsed time meter and to bring up dc power.

   a. If the START switch is not on in the first unit, Sequence Power Out in the second drive has a continuous path through Sequence Power In, K1 (first drive) START switch, Pick Out (first drive) to Pick In (second drive) to energize its K1. In turn, Hold In applies a holding current to the second drive's K1. This process continues through the remainder of the drives until one is encountered with the START switch on.

   b. For the remainder of the sequence, assume that the first drive has a disk pack installed, that all interlocks are closed, and that the START switch is on. Power cannot be sequenced to the next drive until speed relay K2 closes.

2. With the START switch on, a disk pack installed, all interlocks closed, and +20Y power available, the START indicator is lighted. Now that K1 is closed, the control interlock signal provides the last enable to energize motor relay K3.

3. Closed contacts of K3 cause the following:

   a. +20v enables solid state switch A1Q2, A1Q3, and A1Q4. These switches can now conduct ac power to spindle motor.

   b. Because the motor is stopped, centrifugal switch inside the motor is closed. This provides a ground enable to A1Q4 to connect the start winding and capacitor to ac power. At 2,000 rpm the switch transfers to open, disconnecting the start winding and enabling run winding.

   c. Apply GND to the frist seek interlock motor. The first seek interlock switch transfers to the not complete (in progress) position.

   d. Removes power from hysteresis brake.

4. When the logic determines that the spindle speed exceeds 3000 rpm, and the first seek interlock delay is complete, speed relay K2 energizes.

5. With relay K2 closed:

   a. +20 vdc is distributed to the read/write logic (Figure 3-2).

   b. Retract relay K5 is energized (Figure 3-4).

6. The transferring contacts of K5 cause the following:

   a. Disconnects the emergency retract capacitor from the voice coil while connecting it to the -16v power supply to allow it to charge to -16 volts.

   b. Connects the power amplifier A2A1 to the positioner so that the logic may control the positioner.

7. The first seek interlock switch mechanically transfers to the complete position upon completion of the interlock motor revolution (15 seconds for first seek delay). This removes the remaining ground to the interlock motor to disable it. It also signals load heads to the logic.

8. Completion of the first seek delay allows the start of the First Seek (load heads) function. The logic commands the positioner to move the carriage forward. Refer to the First Seek discussion for further information.

9. When the heads move into the pack, the heads loaded switch closes. This causes the following:

   a. Provides a control signal to the logic for further loading/unloading sequencing.

   b. Maintains a motor relay K3 enable so that the motor continues to operate if the control interlock opens. This prevents the motor from being shut down until the heads are unloaded.

   c. Energizes relay K6. If any condition occurs where Retract relay K5 opens, K6 continues to apply -16v retract voltage to the voice coil until the heads unload.

   d. Enables the -16v Sense circuit. If the -16v power becomes insufficient (loss of power), the Select Lock is set and Retract relay K5 opens. Relay K5 connects the retract voltage to the voice coil while removing logic control of the voice coil.

Emergency Retract and Data Protection

Certain emergency conditions could occur which require immediate disabling of the write circuits and full retraction of the heads. These conditions are:

1. Loss of ac power, either site power or UNIT POWER circuit breaker.

2. Opening of any of the control interlocks (Figure 3-4).

3. Overheating of spindle motor. If this occurs, the spindle motor thermostat (Figure 3-3) opens: this applies ac across the DRIVE MOTOR circuit breaker coil to open the contacts. Loss of speed (step 4) occurs.

4. Loss of spindle motor speed.

5. Loss of any of the following ac voltages: +20Y, ±9.7, or -16.

If any of these conditions occur, the read/write logic is disabled and the heads are unloaded. Refer to Figure 3-5 for timing of these conditions.

Loss of AC Power

The following events occur upon catastrophic loss of the ac power or opening of either 5v circuit breaker.

1. All dc power supplies drop their outputs to zero and the logic is disabled.

2. All relays open.

3. With K5 open, the normally-closed contacts of K5 (Figure 3-4) provide a path from the emergency retract capacitor A2C2 to the voice coil. This negative voltage pulls the carriage back to its retracted stop.

4. With K2 open, +20 vdc is removed from the read/write logic.

Control Interlock Opening

If the control interlock (Figure 3-4) opens, the heads unload normally as explained in Power Off Sequence. Pressing START to extinguish the indicator opens the interlock

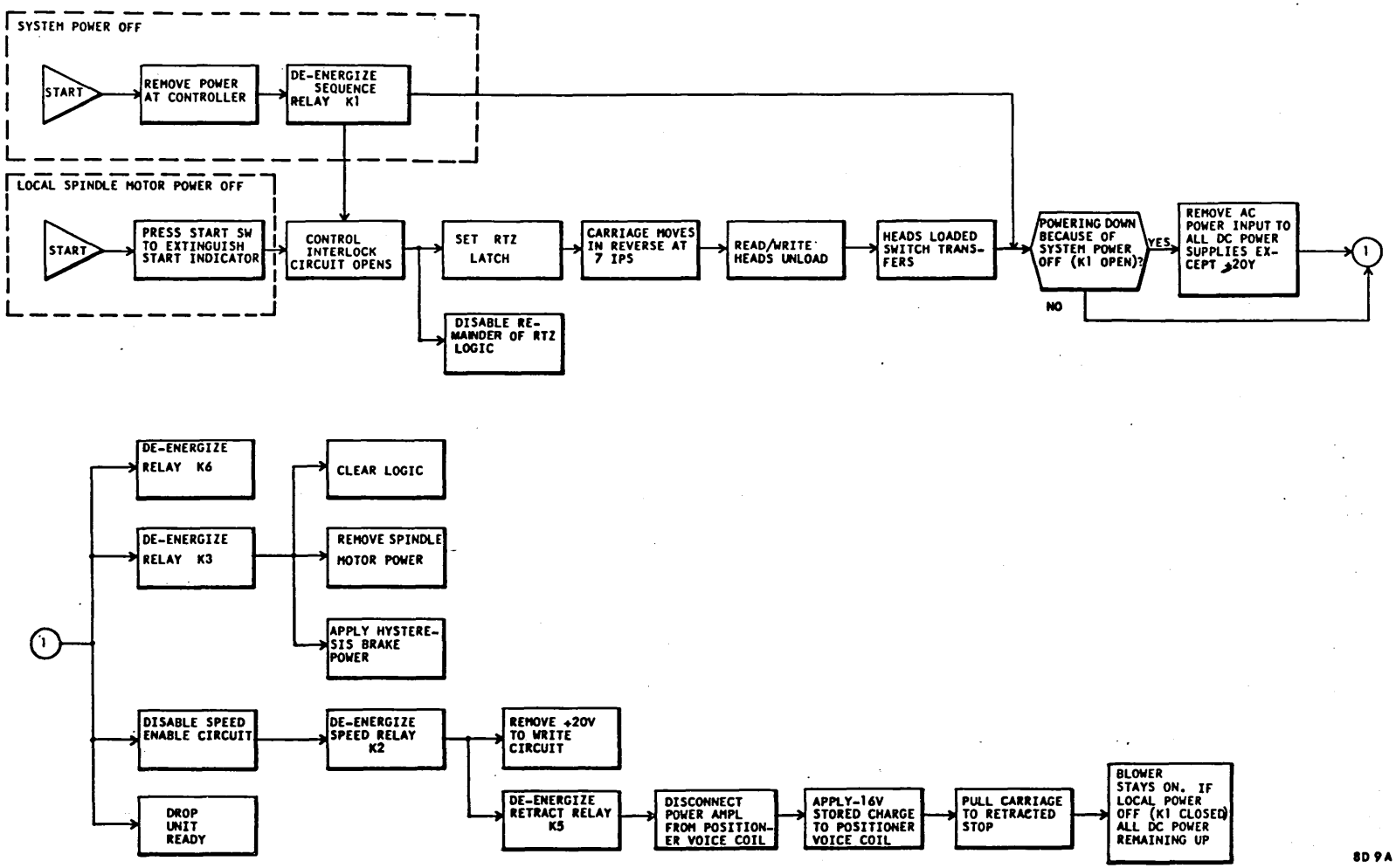


Figure 3-5. Power Off Sequence

to initiate the normal unload heads sequence. There are certain special emergency sensing conditions:

1. If either the +10 or -10 circuit breaker opens, A1Q1 (Figure 3-2) is disabled. The effect is the same as if all ac power were lost. All ac power input to the dc power supplies is opened except to +20Y.

2. Opening a 20v circuit breaker generates an undervoltage condition to set the Select Lock FF and light the SELECT LOCK indicator.

3. Opening of any other circuit breaker or interlock breaks the control interlock.

All of these conditions extinguish the START indicator and unload the heads. Any undervoltage condition (±20v or ±5v) sets the Select Lock FF, and raises bit 0 and bit 3 and/or 4 of Bus In if queried by a Request Diagnostic Sense command bit 5.

Loss of Speed

If the spindle motor speed drops below 2700 rpm, the following events occur:

1. The speed detection circuit in the logic detects the speed loss and opens Speed relay K2. As a backup circuit, when the speed is less than about 2000 rpm, the motor centrifugal switch closes. This breaks the gate in the -16v sense circuit (Figure 3-4)to open K5 and energizes K4 to start a new first seek interlock time delay.

2. With K2 open:

   a. K5 opens to apply -16v retract voltage to the voice coil.

   b. +20 vdc power is removed from the read/write logic.

3. Relay K3 is de-energized when speed drops below 2700 rpm.

4. Relay K6 remains energized to continue to apply -16v retract voltage until the heads retract sufficiently to open the heads loaded switch.

5. When the heads unload, Unit Ready drops.

Loss of DC Power

If +20Y power is lost, all relays open and the ac input to the dc power supplies is opened. The effect is the same as if all ac power were lost.

If +9.7v is insufficient, the following occur:

1. Relays K2 and K3 are opened by the +5v Sense circuit.

2. With K2 open:

   a. K5 opens to apply -16v retract power.

   b. +20v power removed from read/write chassis. With the heads still loaded, the write circuit generates a Current Fault to set the Select Lock FF.

3. With K3 open:

   a. The spindle motor is disabled.

   b. The hysteresis brake is energized.

4. In addition, the undervoltage condition will set the Select Lock FF in the logic; light the SELECT LOCK indicator and raise indicative bits if queried by a Request Diagnostic Sense bit. The condition must be reset to load heads again.

If -16v power is lost, the following occur:

1. The -16v Sense circuit opens K5. It also generates an undervoltage fault condition to set the Select Lock FF.

2. With K5 open, retract power is applied to the voice coil. Since the undervoltage fault has disabled the read/write logic, the circuit is disabled prior to carriage retraction.

3. Relay K5 remains energized, so the drive motor continues to run. Heads cannot load until the SELECT LOCK indicator is cleared.

If ±20v or ±5v power becomes insufficient, the heads do not retract. However, the undervoltage condition sets the Select Lock FF. This has the following effects:

1. SELECT LOCK indicator lights.

2. If heads are not loaded, loading is inhibited.

3. All controller-initiated seeks are inhibited.

4. Read and Write gates are inhibited.

5. During a Request Diagnostic Sense, BOB5, the following bits are up:

a. Bit 0 (Select Lock) and bit 4 (+ volt) for +20v or +5v fault.

b. Bit 0 (Select Lock) and bit 3 (- volt) for -5v or -20v fault.

Power Off Sequence

The normal Power Off sequence begins when the controller opens the sequence power line to the drive. Sequencing is then as follows (see Figures 3-5 and 3-6):

1. Relay K1 de-energizes:

   a. The control interlock opens to raise an Unload Heads command within the logic. This sets the RTZ latch which, in turn,causes the carriage to retract at 7 ips. The carriage performs a normal RTZS, except that the logic that normally stops the carriage at cylinder 000 is inhibited.

   b. Power stays up within the drive because the heads loaded sense function of sensing board A2A3 (Figure 3-4) enables A1Q1 as long as the heads remain loaded.

2. When the heads unload:

   a. Relay K3 de-energizes.

   b. The speed detection circuit is disabled to de-energize relay K2.

   c. Unit Ready drops.

   d. If power is dropped by the system (K1 opens), ac power is removed from the dc power supplies. If power is dropped because START was turned off, however, dc power is not dropped.

3. With K3 open:

   a. The spindle motor is disabled.

   b. Power is applied to the hysteresis brake.

4. With K2 open:

   a. +20v removed from read/write logic.

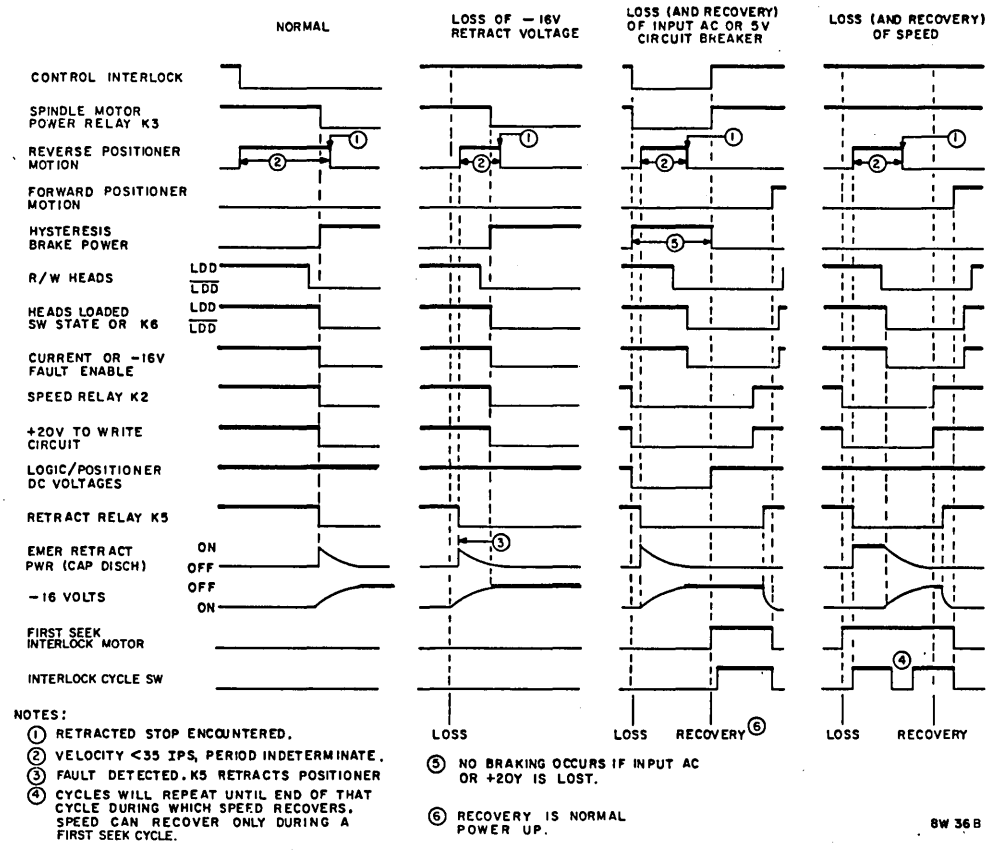


Figure 3-6. Power Off Timing

b. Relay K5 opens. The emergency retract capacitor discharges through the voice coil to pull it back against its retracted stop.

Assuming K1 is open, and with the heads retracted, the +20Y enable is removed from A1Q1 to disable the primaries of T1 and T2. The only dc voltage remaining on is the +20Y required to power up again.

LOGIC CHASSIS

The logic chassis assembly consists of a wire wrap board, logic cards, test point panel, air plenum and dc power supply. The entire assembly forms the rear door to the cabinet. Flexible tubing from the blower assembly connects to the air plenum and provides air to cool the logic cards and the dc power supply.

The logic cards are installed on the protruding pins of one side of the wire wrap board. Wiring between cards and to and from the logic chassis occurs at the protruding pins on the opposite side of the wire wrap board. Access to this wiring is gained by releasing two 1/4-turn fasteners at the top of the door and removing the outer surface of the rear door.

The logic card section contains the bulk of the logic cards used in the cabinet (five cards are located on the deck assembly). The vertically mounted cards are installed in four rows (A top row and D bottom row) at numerically identified locations.

Some cards span two rows and are referred to as full-size cards. Others span a single row and are called half-size cards. Refer to the Diagrams section of the Maintenance manual for a description of the logical functions performed by the cards. The Logic Card manual provides a physical description of the cards. The Wire Lists section of the Maintenance manual contains a tabulation of the wire wrap connections made in the chassis.

The test point panel at the top of the logic chassis provides a convenient point to measure the dc voltages. At the bottom of the logic chassis assembly, and on the front panel of the dc voltage section of the power supply, are located the LOCAL/REMOTE switch, the indicator for +20Y power and the circuit breakers for ±46v, ±20v, and ±10v. Specific information on each control or indicator on the test point and dc power panel is provided in the Operation section of this manual.

DECK ASSEMBLY

The deck assembly mechanism (Figure 3-7) drives the disk pack and loads and positions the read/write and servo heads. The deck assembly consists of a drive motor, hysteresis brake, spindle, actuator, two transducers, and a first seek interlock assembly.

Drive Motor Assembly

The drive motor drives the spindle assembly. The motor is a 3/4-hp unit of the induction type. The motor is secured to a mounting plate. The motor mounting plate is secured to the underside of the deck plate in such a manner as to allow control of belt tension. Power is transferred to the spindle via a flat, smooth-surfaced belt that threads over the pulleys of the spindle and drive motor. Two idler springs maintain a constant tension on the motor mounting plate to keep the belt tight.

A second pulley on the drive motor shaft links the motor (via a V-belt) to the hysteresis brake.

The temperature of the drive motor is monitored by an internal thermostat. If the motor overheats, the thermostat opens. This applies ac across the DRIVE MOTOR circuit breaker coil to open the contacts. The result is a speed loss (refer to Power Supplies). The DRIVE MOTOR circuit breaker must be reset to ON to restore operation.

Hysteresis Brake Assembly

The hysteresis brake decelerates the drive motor during a Power-Off sequence (refer to Power-Off sequence paragraph). The brake is energized whenever Motor relay K3 is de-energized. On units with PE39280B the Hysteresis Brake is attached to the drive motor housing. On units without PE39280B the brake mounts on a plate which, in turn, is mounted on the motor mounting plate; and the brake and motor shafts are linked via a V-belt and a pulley on each shaft.

The brake consists of two concentric permeable bodies. These cylinders are assembled, one inside the other, with a uniform gap separating the outer diameter of one from the inner diameter of the other. These adjacent surfaces are machined to contain a series of pole faces. A permanent magnet, in the shape of a cup, fits in the gap to separate the cylinders. This cup is connected to the drive motor shaft directly in units with PE39280B and via a V-belt in units without PE39280B. As long as drive

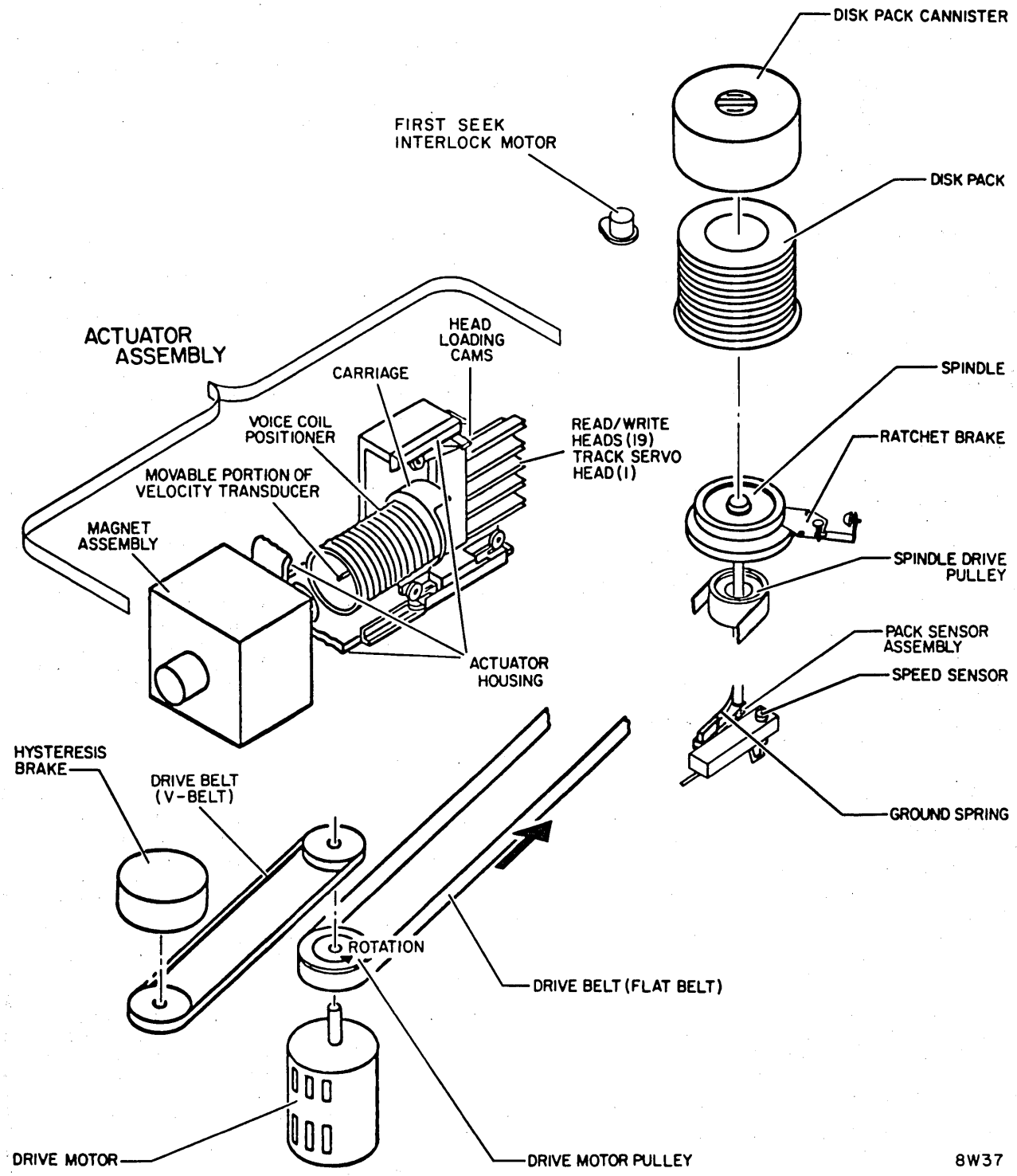


Figure 3-7. Deck Assembly

or spindle motor power is applied, brake power is not available, and the cup is driven at the speed of the motor. When drive or spindle power is removed, braking power is applied. A flux field is created between the inner and outer cylinder pole faces as braking voltage (±20 volts) is applied to the inner cylinder. The flux field sets up what is in effect magnetic friction between the inner cylinder and the cup, causing the cup (and motor) to decelerate.

Spindle Assembly

The spindle assembly is the physical interface between a drive and a disk pack. The surface of the pack mounting plate (Figure 3-8) mates directly with the center of the disk pack.

A vertically free-floating lockshaft runs through the center of the spindle assembly. The upper end of the lockshaft contains internal threads that engage the external threads of a stud projecting from the disk pack. When the disk pack canister cover handle is rotated clockwise, the spring-loaded lockshaft is pulled upward and the disk pack is pulled down. As a result, the mating surfaces of the disk pack and spindle are engaged by a force of approximately 325 pounds. When the disk pack is fully engaged, a release mechanism in the canister handle frees the canister from the disk pack.

The spindle is locked by the pack canister when installing or removing a disk pack.

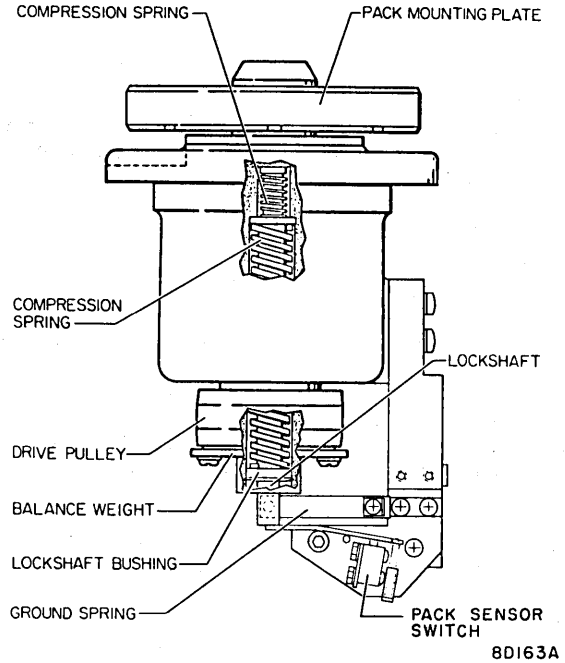


Figure 3-8. Spindle Assembly

This makes it easier to install or remove a disk pack by preventing spindle rotation. The pack on switch and ground spring (Figure 3-8) are mounted at the lower end of the spindle assembly. The ground spring is mounted so that it is always in contact with the lockshaft to bleed off any accumulation of static electricity on the spindle to the deck through a ground strap. The pack on switch contacts transfer in response to the vertical movement of the lockshaft. When the shaft is up (disk pack mounted), the contacts are closed. When a pack is not installed, the shaft moves downward to deflect the switch actuator and transfer the contacts. The switch is part of the interlock that inhibits spindle motor power to an improperly configured unit.

Actuator

The actuator consists of the carriage, actuator housing, and magnet assembly. The actuator (Figure 3-9) is the device that supports and moves the read/write and track servo heads. The forward and reverse moves of the carriage on the carriage track are controlled by a servo signal. The basic signal is developed in the logic section and processed by a power amplifying stage in the power supply. The power amplifier output is applied to the voice coil positioner (part of carriage). The signal causes a magnetic field about the voice coil positioner. This magnetic field reacts with the permanent magnetic field existing around the magnet assembly. The reaction either draws the voice coil into the permanent magnet field or forces it away. Signal polarity determines the direction of motion, while signal amplitude controls the acceleration of the motion.

The voice coil positioner is a bobbin-wound coil that is free to slide in and out of the forward face of the magnet assembly. Fastened to the positioner is a head/arm receiver which holds the 19 read/write heads and the single track servo head. The head/arm receiver mounts on the carriage and bearing assembly that moves along the carriage track on eight bearing type rollers. Movement of the positioner in or out of the magnet causes the same motion to be imparted to the entire carriage assembly. This linear motion is the basis for positioning the read/write and track servo heads to a particular track of data on the disk pack. (Refer to Head Loading paragraph for detailed information on read/write head loading and unloading.)

The positioning signal is derived in the logic chassis and power supply. The signal is applied to the voice coil positioner via two flexible, insulated, metal straps, the ends of which are secured to the cam mount and the carriage and bearing assembly.

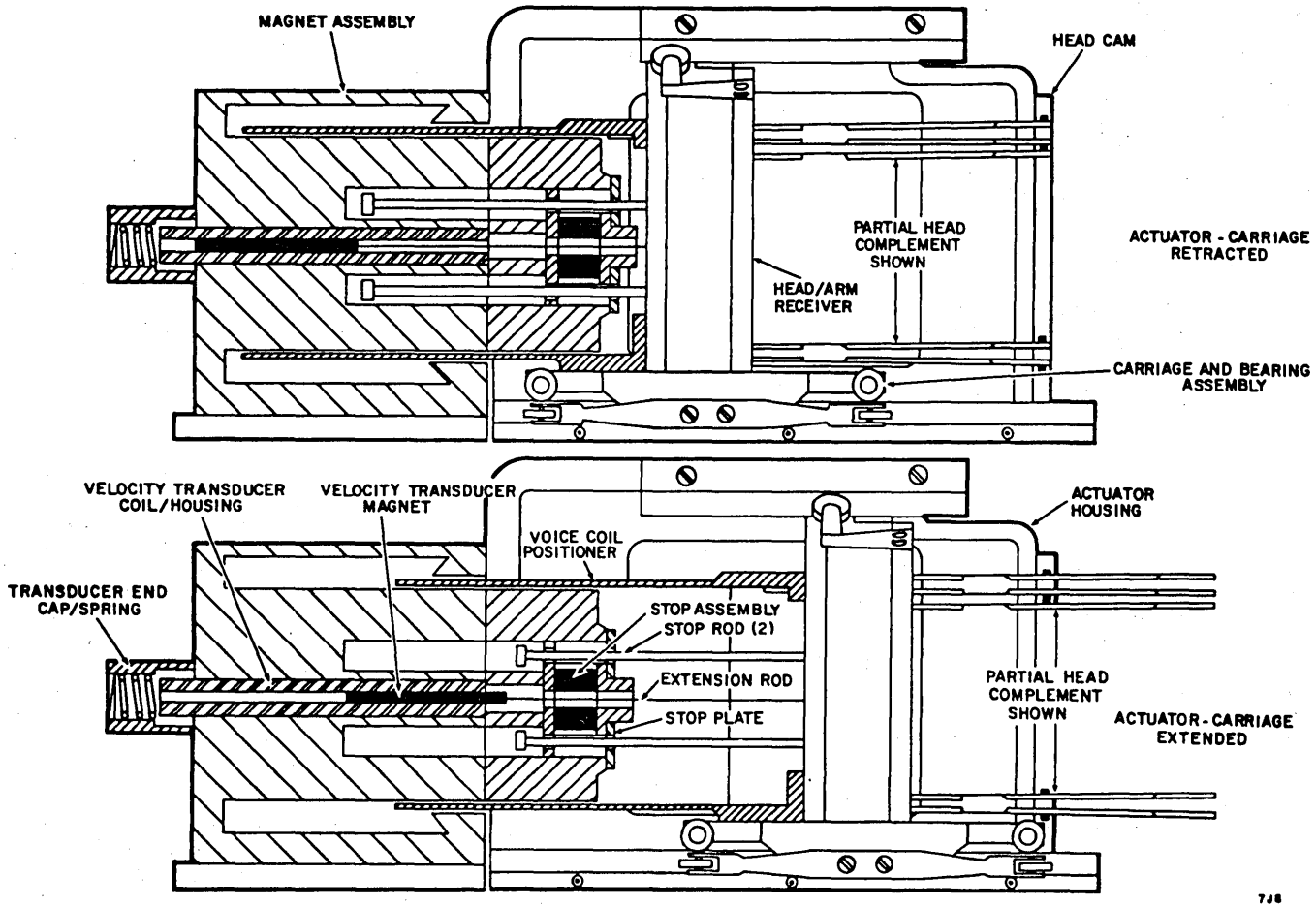


Figure 3-9. Actuator Assembly Elements

During any Seek operation, the logic must be informed of the current location and velocity of the carriage. This information is provided by the velocity transducer in the magnet assembly and the lone track servo head installed on the head/arm receiver. The transducer is a two-piece device, one piece stationary and the other movable. Refer to the Transducers paragraph for a complete description.

The actuator contains a stop mechanism to limit extremes in forward and reverse movement. The stop assembly is a rubber cylinder sandwiched between two metal plates. If the carriage moves too far toward the disk pack, the stop rod heads contact the plate on the magnet-side of the rubber cylinder. If the carriage is retracted far enough away from the disk pack, the rear of the head/arm receiver contacts the stop assembly stud protruding through the stop plate.

Head Loading

The read/write heads must be loaded to the disk surfaces before exchanging data with the controller. The heads must be removed (unloaded) from this position and driven clear of the disk pack either when power is removed from the unit or when the disk pack velocity falls below about 2700 rpm. The actuator components involved in these operations are identified in Figure 3-10.

Head loading amounts to allowing spring pressure of the floating arm (part of head/

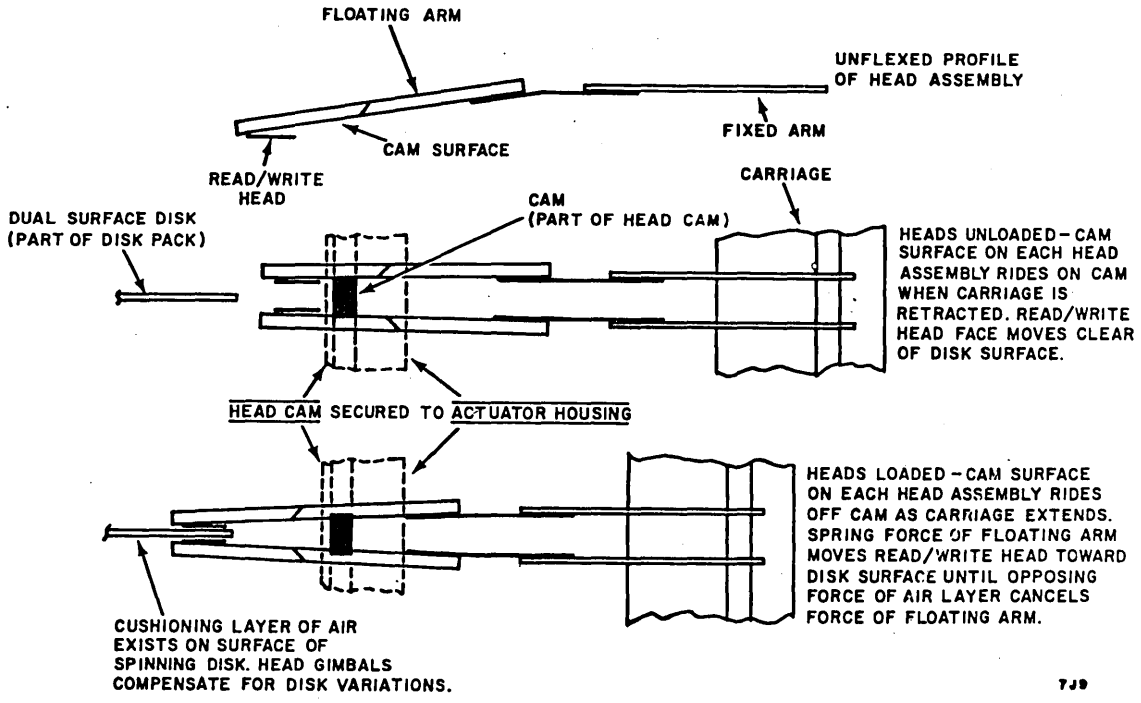


Figure 3-10. Head Loading

arm assembly) to move the aerodynamically shaped head face toward the related disk surface. When the cushion of air that exists on the surface of the spinning disk is encountered, it resists any further approach by the head. Spring pressure is designed to just equal the opposing cushion pressure (function of disk pack rpm) at the required height. As a result, the head flies. However, if the spring pressure exceeds the cushion pressure (as would happen if the disk pack lost enough speed), the head stops flying and contacts the disk surface. This could cause damage to the head as well as the disk surface.

To prevent damage to the heads and/or the disk pack during automatic operation, loading occurs only after the disk pack is up to speed and the heads are over the disk surfaces. For the same reason, the heads unload automatically and are retracted if the disk pack rpm drops out of tolerance. During manual operations, heads should never be loaded on a disk pack that is not rotating. Head loading is part of the Power On/First Seek function. As power to the deck is sequenced up, the drive motor starts. This initiates disk pack rotation and a first seek interlock delay. Actual delay is approximately 15 seconds.

When the disk pack rpm reaches 3000, the power supply speed relay energizes to establish the ability to continue the operation. Upon completion of the first seek interlock delay, the logic specifies a forward seek and the carriage moves forward toward track 0. Head loading occurs during this forward motion. The carriage continues toward the spindle until the servo detects track 0.

The floating arm (Figure 3-10) is designed to maintain a constant loading force. While the heads are retracted, head cams on the actuator housing bear against the floating arm cam surfaces. The cams support the loading force and hold the heads in unloaded position. As the carriage moves forward, the floating arm cam surface rides off the head cam just after the read/write heads move out over the disk surface. The loading force moves the head face toward the air layer on the surface of the spinning disk until the opposing forces balance.

The heads loaded switch status reflects the state of the read/write heads (loaded or unloaded). This status is used in the logic chassis and power supply. The switch mounts on the carriage track and is transferred by carriage motion. Whenever the carriage is

fully retracted, the switch state reflects the unloaded status of the heads. As the carriage moves forward during a Power On/ First Seek, the switch transfers at a point within about 0.1 to 0.2 inch forward of the retracted stop. This switch status remains unchanged until the carriage is retracted to the same position and, as such, does not precisely indicate the loaded/unloaded status of the heads. Precise status is determined by the logic when the servo track head senses dibits.

Head unloading occurs whenever power to the unit is removed or disk pack rpm drops below tolerance. Either event drops a speed enable signal to the logic. This causes the voice coil to drive the carriage in reverse from its current location toward the retracted stop. (Either normal or emergency methods can be used. Refer to Power Off Sequence paragraph for additional information.) As the carriage retracts, the cam surfaces encounter the head arms and each head rides vertically away from the related disk surface. The carriage continues back to the retracted position and stops.

Head/Arm Assemblies

Twenty head/arm assemblies are mounted on the carriage. A read/write head/arm assembly consists of a read/write head assembly mounted at the end of a supporting arm structure. A track servo head/arm assembly consists of a read coil head assembly mounted at the end of a supporting arm structure.

The head assembly (Figure 3-11), which includes a cable and plug, is mounted on a gimbal ring which, in turn, is mounted on a floating arm. This method of mounting allows the head assembly to pivot (independent of the arm) tangentially and radially relative to a data track on the disk surface. Such motion is required to compensate for possible irregularities in the disk surface.

The arm structure consists of a floating arm secured to a heavier fixed arm. The end of the fixed arm opposite the head mounts in the carriage receiver. The floating arm is the mounting point for the head and is necessarily flexible so that it can flex during load and unload motions, onto and off of the cam surfaces.

Freedom and mobility of the head are necessary elements to being able to function with interchangeable disk packs. During head loading, each floating arm is driven off the related cam and unflexes to force a head toward the air cushion on the spinning disk surface. The force applied by the floating arm causes the heads to fly or float on the air cushion. Vertical motion by a disk surface (due to warpage or imperfection) is

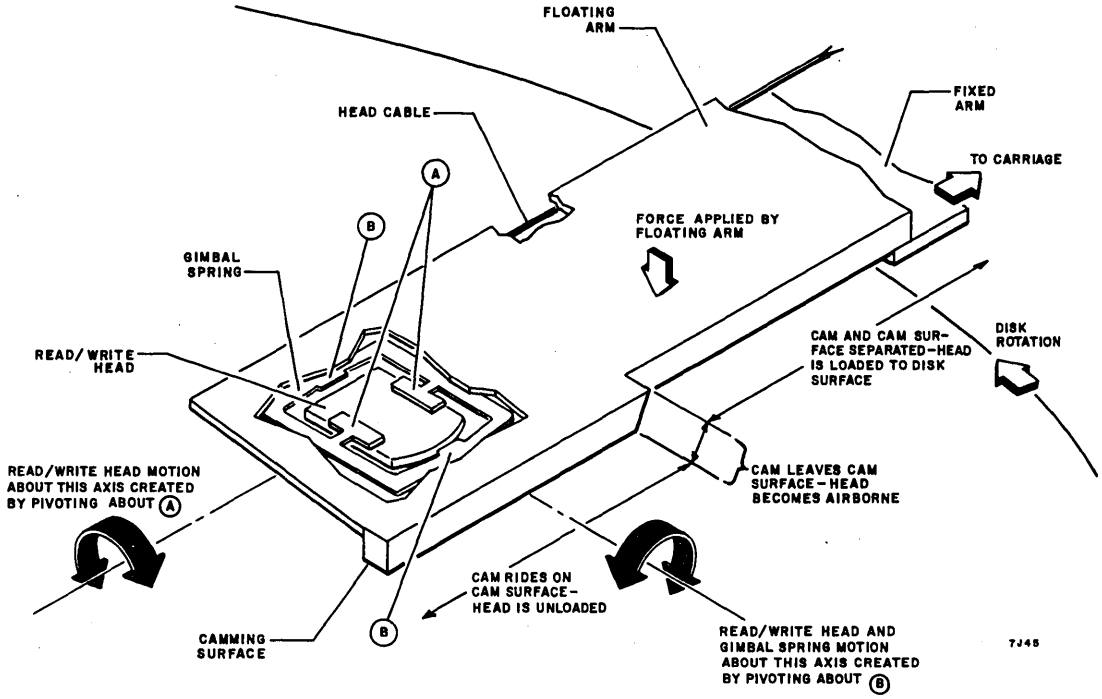


Figure 3-11. Head/Arm Assembly Motion

countered by a move in the opposite direction by the gimballed head and/or floating arm. As a result, flight height remains nearly constant.

Transducers

The deck assembly contains two transducers: speed sensing transducer and velocity transducer. These transducers provide signals that are used by the logic chassis and the controller to generally control the progression of most machine operations.

Speed Sensing Transducer

The speed sensor (Figure 3-7 and 3-12) generates a voltage output whenever a ferrous material (steel pin set in spindle pulley) enters the magnetic field surrounding the pole piece at the pickup end of the transducer. The logic then shapes this signal into a 55 microsecond pulse. As long as the speed exceeds 3000 rpm, one of these pulses will be sensed at least once each 20 ms. A sensing circuit within the logic monitors the pulse repetition rate and provides an enable to Speed relay K2.

If speed is insufficient, the pulse repetition rate is reduced accordingly. This has either of two effects:

1. If the heads are not loaded, K2 cannot energize and the logic will not initiate the load sequence.

2. If the heads are already loaded, K2 opens, thereby opening the coil of Retract relay K5. The voice coil is disconnected from the logic power amplifier and connected to the -16v emergency retract capacitor. The heads immediately are unloaded to the retracted stop.

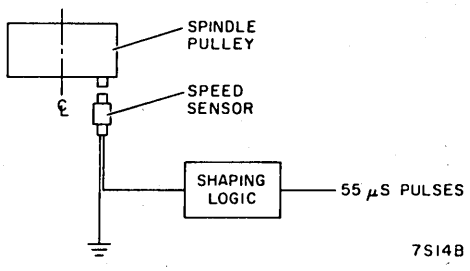


Figure 3-12. Speed Detection

Velocity Transducer

The velocity transducer (Figure 3-13) is a two-piece device consisting of a stationary tubular coil/housing and a movable magnetic core.

The magnetic core is connected via the extension rod to the rear surface of the head/arm receiver. All motion of the carriage is therefore duplicated by the magnetic core. As the core moves, an emf is induced in the coil. The amplitude of this emf is directly related to the velocity of the core (and carriage). The polarity of the emf is an indication of the direction of movement by the core (and carriage). The transducer output drives an operational amplifier located in the logic chassis. This signal is used by the servo logic to control acceleration/deceleration of the carriage during Seek operations.

First Seek Interlock Assembly

The First Seek Interlock assembly provides a fixed time delay from the completion of the Start interlocks until heads can be loaded during the Power On/First Seek sequence.

The assembly consists of a motor, reset switch, cam linkage, and a mounting base. The base mounts on the deck assembly. The motor is energized during the Power On sequence and starts a 15-second (approximate) first seek interlock delay cycle. The cam revolves until the reset switch is encountered. The switch then transfers and removes power to the motor and signals completion of the delay cycle to the logic.

If power is lost or dropped during the cycle, the cam completes the initial cycle upon reapplication of power. At this time, a new cycle is initiated if Speed relay K2 has not been energized. Refer to Power On paragraph for a complete description of conditions that apply power to the first seek interlock motor.

BLOWER SYSTEM

The blower system (Figure 3-14) provides positive pressure in the pack area. The presence of this elevated pressure results in an outward dispersion of air preventing ingestion of contaminated air. This air flow greatly reduces possible contamination and resulting damage to the disk surfaces and the read/write heads.

Power to the blower drive motor is available whenever the UNIT POWER circuit breaker is on.

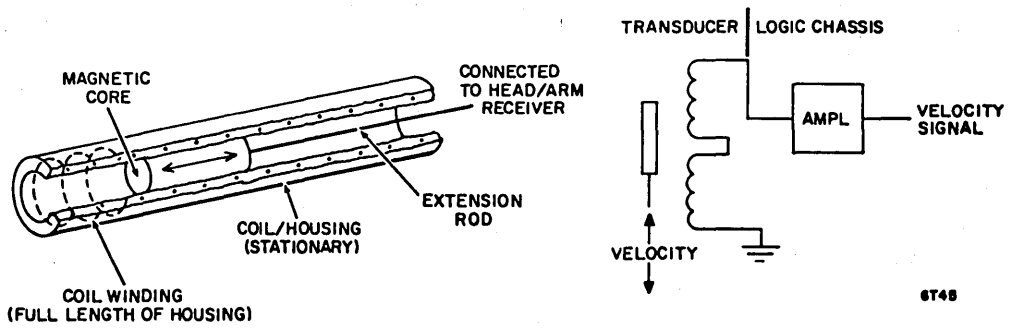


Figure 3-13. Velocity Detection

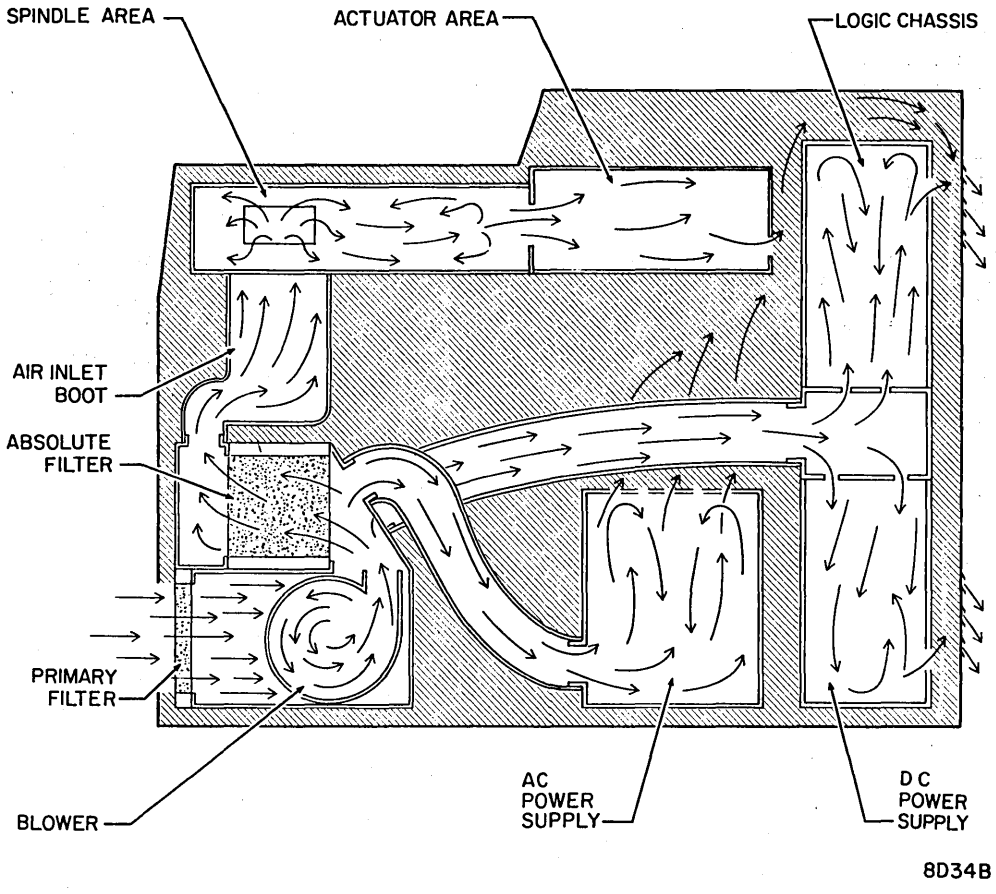


Figure 3-14. Blower System

DISK PACK

The disk pack is the recording medium for the drive. The disk pack consists of 12 14-inch disks, center-mounted on a hub. The recording surface of each disk is coated with a layer of magnetic iron oxide and related binders and adhesives. The top and bottom disks are protective non-recording disks.

There are 19 recording surfaces and one track servo surface. The servo disk contains pre-recorded information that is used by the servo logic to position the heads to the desired track.

The 823 recording tracks (0-822) are grouped in a 2-inch band near the outer edge of the disk. Track 822 has a diameter of approximately 9 inches, while the diameter of track 0 is about 13 inches. The tracks are spaced about 0.0026-inch apart.

The disk pack has a two-piece container. The bottom cover can be removed simply by grasping and rotating the center hub. The top cover is designed so that it can be removed only by installing the disk pack on the spindle. The disk pack can be removed from the spindle only by using the top cover (see Operation section). This design protects the disk pack from physical damage and greatly reduces the possibility of contamination of the disk pack recording surfaces.

LOGIC FUNCTIONS

The logic functions performed by the drive are subdivided as follows:

- Basic Interface Description
- Unit Selection
- Seek Operations
- Diagnostic Operations
- Basic Read/Write Principles
- Write Operations
- Read Operations

Most operations require the transfer of data between the controller and the drive. Descriptions of these signal interchanges will emphasize drive functions. Controller functions are described only where necessary to clarify drive operations. Unless otherwise specified, controller signal timing is for illustrative purposes only. Refer to the applicable controller manual for details of controller operations and actual I/O timing.

BASIC INTERFACE DESCRIPTION

Figure 3-15 is a block diagram of the drive and its I/O lines. The block diagram shows only the main elements involved in the I/O dialog. More detailed diagrams that illustrate signal interchange between drive logic subsystems are provided in the applicable theory portion of this manual.

Signals are exchanged between the controller and drive by two signal cables. These cables are the "A" (Control and power sequence) cable and the "B" (Data and PLO signal) cable. The "A" cable is a twisted pair cable containing 104 lines. The "B" cable contains shielded balanced lines. Dual channel units have a pair of cables for each controller.

Definitions of the signals on the I/O lines are provided by Table 3-1. Table 3-2 defines the meanings of the bits on the bus lines in accordance to the active tag.

UNIT SELECTION

The drive must be selected before it can accept any commands from the controller. There is one case where the drive can communicate with the controller without previous selection (Poll Devices) but the drive must be selected before any further operation can take place.

The unit is selected when the Module Select Gate line goes high, Tag 3 Bus Out Bits 7, 6, and 5 match the LAP decode, and parity is odd. The unit is selected and available for further commands from the controller as long as Module Select Gate remains high. While selected the drive physical address code is transmitted to the controller on six lines using a three of six code.

Bus In Bit 6 when active, defines the unit as a 200 megabyte capacity unit.

SEEK OPERATIONS

Seek operations are those drive functions that cause a repositioning of the read/write heads. The heads are attached to the actuator which, in turn, is moved by a voice coil positioner. The mechanical elements involved in the mechanism are described in the assembly portion of this section.

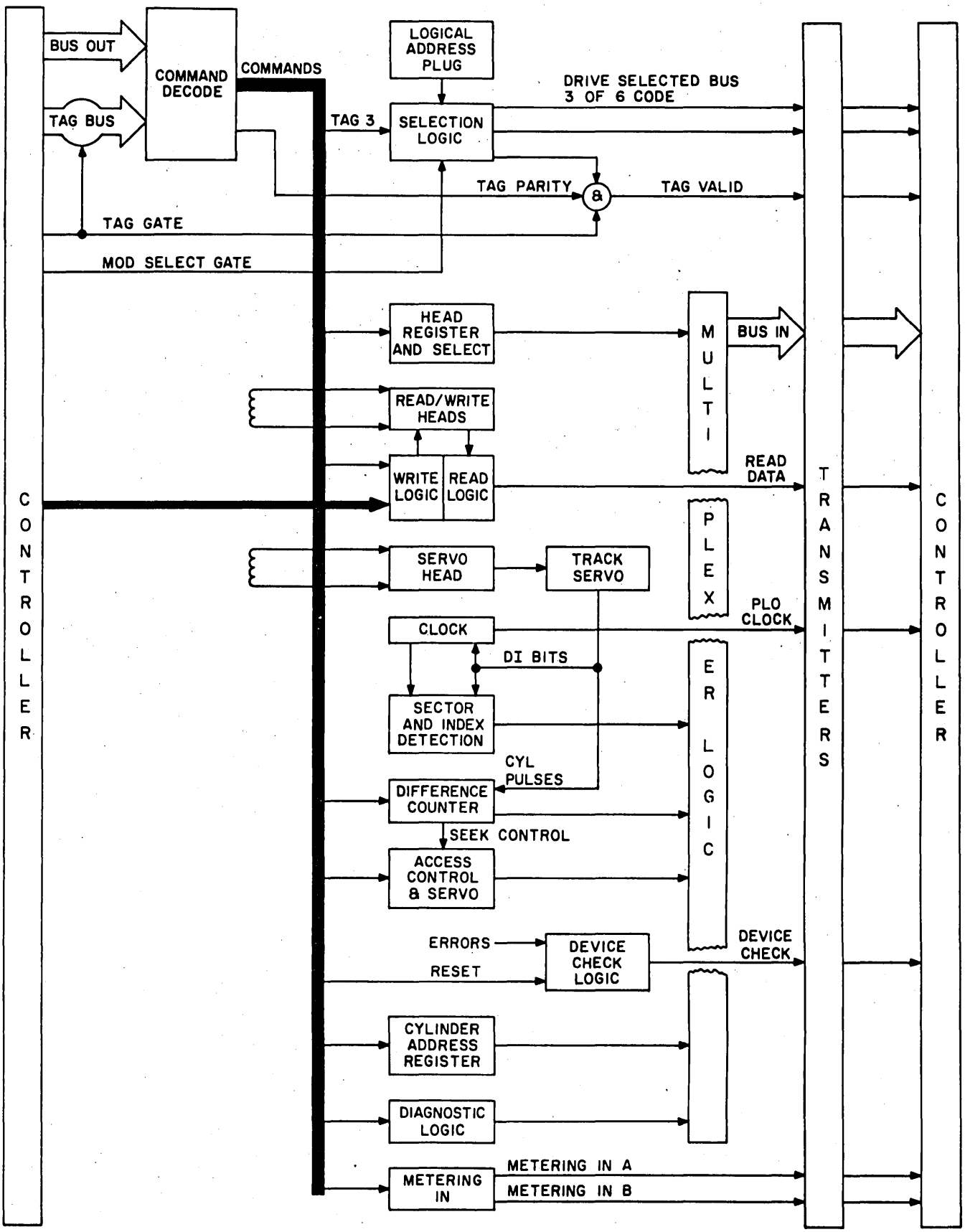


Figure 3-15. Logic Block Diagram

8D80

TABLE 3-1. I/O LINES

Source	Signal Name	Function
		"A" CABLE LINES
Controller	Tag Bus Lines	Four lines plus parity that define operation to be performed by drive. Decoded in drive to define Tag functions.
Controller	Tag Gate	Gates Tag Bus signals into drive. Odd parity on Tag Bus is maintained during time Tag Gate is high.
Controller	Bus Out (BO)	Eight bits plus parity that supply control signals to the drive. Meaning of the signals is a function of the active tag lines.
Controller	Module Select Gate	Used with Tag Decode 3 to select a drive when the drive has decoded a valid logical address.
Controller	General Reset	Clears all reserved latches of drives not selected.
Controller	Controller On Power (COP)	Transmits a -12v signal to drive when controller power is on. Enables interface receivers of this channel.
Controller	Power Up Sequence Line	A ground on this line activates the Power Sequence in the drive.
Drive	Drive Selected Bus	Six lines which return drive units "3-of-6" code to controller when drive is selected. Codes are as follows:
Drive	Bus In (BI)	Eight lines plus parity that supply information signals to the controller. Meaning of bits is a function of the Tag Bus lines from the controller.
Drive	Tag Valid	This line indicates a Tag Bus signal, Tag Gate and correct parity has been received.
Drive	Metering in A	Active when unit is on line, a seek or restore is in process and Tag 9-BOB1 was not activated after last Seek Complete or Record Ready interrupt. This line is also active during a Record Search operation until the first Record Ready interrupt is detected. (This line is not used by the controller.)

Drive Location	Bits 2	3	4	5	6	7
A	1	1	1	0	0	0
B	1	1	0	0	0	1
C	1	0	1	0	1	0
D	1	0	0	0	1	1
E	0	1	1	1	0	0
F	0	1	0	1	0	1
G	0	0	1	1	1	0
H	0	0	0	1	1	1

TABLE 3-1. I/O LINES (CONT'D)

Source	Signal Name	Function
Drive	Metering in B	Active when unit is on line, a seek or restore in process and Tag 9-BOBl was active after last Seek Complete or Record Ready interrupt. This line is also active during a Record Search operation until the first Record Ready interrupt is detected. (This line is not used by the controller.)
Drive	Device Check	Signals that a drive recognizable error has occurred in the selected drive. Drive recognizable errors are: 1. (Seek Incomplete) AND (Offset Reset OR Offset Start) 2. Start Seek and (Offset Active OR Seek Incomplete OR Not On Cylinder) 3. Diagnostic 1 and (Offset Reset OR Offset Start OR Return to Zero Seek OR Start Seek) 4. Operate Tag (Tag 11) and (Not On Cylinder OR Diagnostic 1) 5. Select Lock latch set by: a. Write and No Write Current, or b. Not Write and Write Current, or c. Multiple Heads Selected, or d. Write Overrun, or e. Write and Offset, or f. Read and Write, or g. Voltage Faults, or h. No Servo Tracks, or i. Loss of AC Write Transitions j. Write and Not On Cylinder k. Write Gate and No Head Selected 6. Head Advance and End of Cylinder 7. Interface Check 8. Monitor Check 9. Test Logic
Drive	DIP (Device On Power)	Transmits a -12v signal to the controller when unit power is on. This signal is used in the controller to open its interface line receivers for this unit.
	"B" CABLE LINES	
Controller	Write Data	Transmits modified frequence modulation (MFM) data to be recorded on the disk pack. Bit rate is 6.451 MHz.
Drive	Read Data	Transmits detected digital MFM data.
Drive	PLO Clock	Transmits 806.4 kHz digital pulse train derived from the disk pack servo track.

TABLE 3-2. TAG DECODE AND CONTROL BUS FUNCTIONS

Tag No. & Name	Notes and Function
1 Transmit Sector	1. Unit must be selected. 2. Sets Sector Register to a value determined by BOB1-B7. 3. Turns on the Record Search Latch. 4. Causes Record Ready interrupt (see Tag 2 below) to be activated when the Sector Counter value equals the Sector register. The Interrupt signal drops when sector count advances. It is reactivated each disk revolution until serviced.
2 Poll Devices	1. Unit need not be selected. 2. Causes unit with interrupt condition to place its Logical Address Plug (LAP) decode bit on BI. Interrupt conditions are: attention latch on, Seek Complete Interrupt, Seek Incomplete Interrupt and Record Ready Interrupt. 3. Tag 2 BOB7 polls units 0-7. 4. Tag 2 BOB5 polls Service unit.
3 Transmit Module Address	1. Selects unit by turning on Selected latch if: BOB7, B6 and B5 match the LAP decode (BOB3 selects Service), Module Select Gate is high. 2. BIB6 is returned to controller if unit is a 200 megabyte unit.
4 Request Status	1. Unit must be selected. 2. Byte on Bus In returns status information to controller as follows: BIB Name / BIB Name 0 Index Error / 4 On Line 1 Offset Active / 5 Attention 2 Seek Incomplete / 6 Busy 3 Seek Complete / 7 Record Search in Progress 3. Bus Out Byte is not significant unless Tag 13 BOB2 (Diagnostic Mode 2) is set. In this case, the Bus Out bits command various drive operations as follows: BOB Command 0 Simulate Even Dibit 1 Simulate Forward EOT Enable 2 Simulate Reverse EOT Enable 3 Simulate Velocity 4 Blank On Cylinder 5 Simulate Fine Enable 6 Inhibit Unload Heads and Simulate Heads Loaded
5 Request Address	1. Unit must be selected. 2. Gates the contents of various registers to BI depending on the BO byte present as follows:

TABLE 3-2. TAG DECODE AND CONTROL BUS FUNCTIONS (CONT'D)

Tag No. & Name	Notes and Function
5 (Cont'd)	BOB3 - Read Difference Counter BIB 0 Difference Count 128/Offset Reverse 1 Difference Count 64/Sign Change 2 Difference Count 32 3 Difference Count 16/400 µin Offset 4 Difference Count 8/200 µin Offset 5 Difference Count 4/100 µin Offset 6 Difference Count 2/50 µin Offset 7 Difference Count 1/25 µin Offset BOB6 - Read High Difference BIB 0 Diff 512 1 Diff 256 4 Reverse BOB4 - Read Head Address Register BIB Head Address Register No. 0 CAR 512 1 CAR 256 3 16 4 8 5 4 6 2 7 1 BOB5 - Read Cylinder Address Register BIB Cylinder Address Register No. 0 128 1 64 2 32 3 16 4 8 5 4 6 2 7 1 BOB7 - Read Sector Register BIB 0 High Side of Sector 1 Sector 64 2 Sector 32 3 Sector 16 4 Sector 8 5 Sector 4 6 Sector 2 7 Sector 1

TABLE 3-2. TAG DECODE AND CONTROL BUS FUNCTIONS (CONT'D)

<table>
<tr><th>Tag No. & Name</th><th>Notes and Function</th></tr>
<tr><td>5 (Cont'd)</td><td>A Read Sector Register command may be used with a Save Sector operation as follows:

Save Sector (Tag 11 BOB7) sets the Sector register to the value in the sector counter at the time of the Save Sector command. The Read Sector Register command then places the sector counter value on Bus In. If the clock count within the sector has reached 23, bit 0 in the sector count byte is set to a "1". If the Save Sector command does not occur before count 50 in any sector, the sector count transfer is delayed until count 4 of the next sector and the sector number of the next sector is transferred.</td></tr>
<tr><td>6
Transmit Cylinder Address</td><td>1. Unit must be selected.
2. Normal operation is to:
a. Set the CAR according to Bus Out Byte.
b. Reset the difference register to the highest value.
c. Reset the direction latch to forward.
d. Reset the HAR to head zero.
3. For normal operation to occur, the following conditions must be met:
a. Command Valid
b. No Device Check and (Diagnostic Mode 1 latch off or Diagnostic Mode 2 on)
c. On Cylinder or Diagnostic Mode 2 on
4. Regardless of whether normal operation is allowed or not,Tag 6 active causes the present value of the CAR to be placed on the Bus In lines to the controller.
5. Bus In and Bus Out Byte decode is:

<u>Bit</u> <u>Decode</u>
0 CAR 128
1 CAR 64
2 CAR 32
3 CAR 16
4 CAR 8
5 CAR 4
6 CAR 2
7 CAR 1</td></tr>
<tr><td>7
Transmit Head Address</td><td>1. Unit must be selected.
2. Normal operation is to set the HAR latch to the value of Bus Out as follows:

<u>BOB</u> <u>Decode</u> <u>BOB</u> <u>Decode</u>
7 HAR 1 3 HAR 16
6 HAR 2 2 Not used
5 HAR 4 1 CAR 256
4 HAR 8 0 CAR 512

3. For normal operation to occur the same conditions as those for enabling normal operation of Tag 6 and 10 must be present.</td></tr>
</table>

TABLE 3-2. TAG DECODE AND CONTROL BUS FUNCTIONS (CONT'D)

<table>
<tr><th>Tag No. & Name</th><th>Notes and Function</th></tr>
<tr><td>7 (Cont'd)</td><td>
4. In all cases, Tag 7 causes the following bits to be gated to Bus In.
<table>
<tr><th>BIB</th><th>Decode</th><th>BIB</th><th>Decode</th></tr>
<tr><td>7</td><td>HAR 1</td><td>3</td><td>HAR 16</td></tr>
<tr><td>6</td><td>HAR 2</td><td>2</td><td>Not used</td></tr>
<tr><td>5</td><td>HAR 4</td><td>1</td><td>CAR 256</td></tr>
<tr><td>4</td><td>HAR 8</td><td>0</td><td>CAR 512</td></tr>
</table>
</td></tr>
<tr><td>8
Transmit
Difference/Offset</td><td>
1. Unit must be selected.
2. Under the same conditions as required for Tags 6,7,and 8, the difference counter is set according to the bits on Bus Out.
<table>
<tr><th>BOB</th><th>Diff Counter</th><th>BOB</th><th>Diff Counter</th></tr>
<tr><td>0</td><td>128</td><td>4</td><td>8</td></tr>
<tr><td>1</td><td>64</td><td>5</td><td>4</td></tr>
<tr><td>2</td><td>32</td><td>6</td><td>2</td></tr>
<tr><td>3</td><td>16</td><td>7</td><td>1</td></tr>
</table>
3. In all cases, Tag 8 gates the difference counter output to Bus In.
4. Tag 8 also determines the amount of offset of the Read/Write heads from the track center line when the Tag 8 command is followed by an Offset Start command (Tag 9 BOB2). In this case, offset direction and amount is set as follows:
<table>
<tr><th>BOB</th><th>Tag Decode</th><th>BOB</th><th>Tag Decode</th></tr>
<tr><td>0</td><td>Reverse</td><td>4</td><td>200 µinches</td></tr>
<tr><td>1</td><td>Sign Change</td><td>5</td><td>100 µinches</td></tr>
<tr><td>2</td><td>Not Used</td><td>6</td><td>50 µinches</td></tr>
<tr><td>3</td><td>400 µinches</td><td>7</td><td>25 µinches</td></tr>
</table>
</td></tr>
<tr><td>9
Transmit Control I</td><td>
1. Unit must be selected.
2. Gates the same byte to Bus In as Tag Decode 4 (Request Status).
3. Performs logic control functions according to Bus Out bits 0-7 as follows:
<table>
<tr><th>BOB</th><th>Function</th></tr>
<tr><td>1</td><td>Enables Metering in B.</td></tr>
<tr><td>2</td><td>Activates Offset Start. Amount and direction of offset is specified Tag 8 BOB 0-7.

Device Check is turned on if Offset operation can not be performed. The following conditions prevent Offset Start.

a. Power On Reset
b. Seek Incomplete
c. Not On Cylinder
d. Not On Line
e. Diagnostic 1 Active</td></tr>
</table>
</td></tr>
</table>

TABLE 3-2. TAG DECODE AND CONTROL BUS FUNCTIONS (CONT'D)

<table>
<tr><th>Tag No. & Name</th><th>Notes and Function</th></tr>
<tr><td>9 (Cont'd)</td><td>
<table>
<tr><th>BOB</th><th>Function</th></tr>
<tr><td>3</td><td>Seek Start. Heads are moved the number of cylinders specified by the value in the Difference counter. Device Check is turned on if the operation can not be performed.

Conditions which prevent a Seek Start are the same as those which prevent an Offset Start plus - f. Offset Active.</td></tr>
<tr><td>4</td><td>Rezero Start. Returns Heads to cylinder 0. Device Check is turned on if Rezero Start cannot be performed. Not On Cylinder, Not On Line, or Diagnostic 1 active prevent Rezero Start.</td></tr>
<tr><td>5</td><td>Reset Head Address Register - Turns off HAR 1,2,4,8, and 16 latches. Sets HAR to zero.</td></tr>
<tr><td>6</td><td>Control Reset. Performs same function as Power On Reset. Resets:

a. Select Lock
b. Device Check
c. Interface Check
d. Command Reject
e. Current Fault
f. Write Overrun
g. Monitor and Mode Latches
h. Diagnostic Mode Latches</td></tr>
<tr><td>7</td><td>Reset Interrupt. Resets the following interrupt circuits:

a. Sector Register Latches
b. Record Search Latch
c. Attention Latch</td></tr>
</table>
</td></tr>
<tr><td>10
Transmit Control 2</td><td>1. Unit must be selected.

2. Performs logic control functions according to BOB as follows:

<table>
<tr><th>BOB</th><th>Decode</th><th>BOB</th><th>Decode</th></tr>
<tr><td>0</td><td>Diff 512</td><td>4</td><td>Reverse</td></tr>
<tr><td>1</td><td>Diff 256</td><td>5</td><td>Not used</td></tr>
<tr><td>2</td><td>Set High Diff</td><td>6</td><td>Decrement Diff</td></tr>
<tr><td>3</td><td>Reset Diff</td><td>7</td><td>Offset Reset</td></tr>
</table>
3. For normal operation to occur, the following conditions must be met:

a. Command Valid
b. No Device Check and (Diagnostic Mode 1 latch off or Diagnostic Mode 2 on)
c. On Cylinder or Diagnostic Mode 2 on</td></tr>
</table>

TABLE 3-2. TAG DECODE AND CONTROL BUS FUNCTIONS (CONT'D)

<table>
<tr><th>Tag No. & Name</th><th>Notes and Function</th></tr>
<tr><td>10 (Cont'd)</td><td>4. Regardless of whether normal operation is allowed or not, Tag 10 active causes the following bits to be gated to Bus In.

<table>
<tr><th>BIB</th><th>Decode</th></tr>
<tr><td>0</td><td>Diff 512</td></tr>
<tr><td>1</td><td>Diff 256</td></tr>
<tr><td>2,3</td><td>Not used</td></tr>
<tr><td>4</td><td>Reverse</td></tr>
<tr><td>5,6</td><td>Not used</td></tr>
<tr><td>7</td><td>Not used</td></tr>
</table></td></tr>
<tr><td>11
Operate</td><td>1. Unit must be selected, however odd parity is not necessary on Bus Out with Tag 11 to activate Command Valid.

2. Bus Out bits will be active when the Tag 11 Valid line is activated. Tag 11 Valid is active only when all the following conditions exist:

a. No Device Check
b. Diagnostic 1 Latch Off
c. Select Lock Latch Off
d. On Cylinder
e. Command Valid Active
f. Tag Decode 11 Active

3. If Tag 11 can not be performed a Command Reject signal is generated.

4. A Tag 11 Valid signal allows the Bus Out bits to select the operation as follows:

<table>
<tr><th>BOB</th><th>Operation</th></tr>
<tr><td>0</td><td>Start Write Address Mark</td></tr>
<tr><td>1</td><td>Address Mark Search</td></tr>
<tr><td>2</td><td>Data Enable</td></tr>
<tr><td>3</td><td>Select Head - according to HAR</td></tr>
<tr><td>4</td><td>Head Advance</td></tr>
<tr><td>5</td><td>Write</td></tr>
<tr><td>6</td><td>Read</td></tr>
<tr><td>7</td><td>Save Sector</td></tr>
</table>
5. The Bus Out bits may be used in combinations as follows:

<table>
<tr><th rowspan="2">Operation</th><th colspan="8">Bus Out Bits</th></tr>
<tr><th>0</th><th>1</th><th>2</th><th>3</th><th>4</th><th>5</th><th>6</th><th>7</th></tr>
<tr><td>Write Address Mark</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Address Mark Search</td><td>0</td><td>1</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Write Data</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>Read Data</td><td>0</td><td>0</td><td>1</td><td>1</td><td>0</td><td>0</td><td>1</td><td>0</td></tr>
<tr><td>Head Advance</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td><td>0</td><td>0</td><td>0</td></tr>
<tr><td>Save Sector</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>0</td><td>1</td></tr>
</table></td></tr>
</table>

TABLE 3-2. TAG DECODE AND CONTROL BUS FUNCTIONS (CONT'D)

Tag No. & Name	Notes and Function
11 (Cont'd)	The lines remain active until the operation is complete. • Write Address Mark (Tag 11 BOB 0,3,5) . Write the track for three byte times as determined by the controller. . A 5.0 µsec delay is fired which blocks Write Fault. . Bit 0 activates the Start Write Address Mark line. . Bit 3 causes a Head Select. . Bit 5 activates the Write circuit. No clock or data bits are provided to be written. • Address Mark Search (Tag 11 BOB1,2,3,6) . Operation is typically performed during an inter-record gap. . Read operation is in progress, therefore bits 2,3,and 6 are active. . Bit 1 activates the Address Mark Search. Objective is to read until the controller senses it has not received any clock or data pulses for three byte times. • Save Sector (Tag 11 BOB7) . Sets the Sector register to the value in the Sector counter. If clock count has not reached 50 when the Save Sector signal is received, the value in the sector counter is immediately set into the Sector register. If a count of 50 has been reached, the Sector register is set to the value in the sector counter at the next clock count of 4. . The Save Sector operation allows the controller to sense what sector the heads are in by a Tag 5 BOB7 (Request Address, Read Sector). • Read (Tag 11 BOB2,3,and 6) . Bit 3 allows the activation of one of the head select lines in the same manner as in a write operation. . Bit 6 activates Read Select. All the following conditions must be met: a) Tag 11 Valid and Bus Out Bit 6 b) Not Write Gate c) Head Select d) Not Diagnostic Mode 1 latch . Data Enable (Bit 2) gates the outputs of the Read detector to the controller if the following conditions are met: a) Head Select active b) Read active c) Not Write Gate active d) Not Diagnostic Mode 1 Latch on

TABLE 3-2. TAG DECODE AND CONTROL BUS FUNCTIONS (CONT'D)

Tag No. & Name	Notes and Function
11 (Cont'd)	• Head Advance (Bit 4) . Each time bit 4 is brought up it increments the Head Address register. The following conditions must be met: a) Not Head Select (Tag 11 BOB3) b) Not Write (Tag 11 BOB5) c) Not Read (Tag 11 BOB6) d) Not End of Cylinder • Write (Tag 11 BOB3 and 5) . Head Select (Bit 3) must be active to read or write. . Head Select blocks Head Advance. Head Select can not be activated if the Diagnostic Mode 1 latch is on. . Write (Bit 5) causes the Clock and Data pulses from the controller to be written if the following conditions are met: a) Head Select (Tag 11 BOB3) active b) Ready c) Not offset
12 Request Diagnostic Sense	1. Unit must be selected. 2. Functions performed depend on which bus out lines are active. BOB 1 Gates Servo Points to the Bus In as follows: BIB0 Desired Velocity greater than 128 1 On Cylinder 2 Fine Analog 3 Difference Count = 0 4 Fine Mode 5 Dibits 6 Cylinder Pulse 7 EOT 2 Gates Status of Monitor Mode and diagnostic mode latches to the bus in as follows: BIB0 Not used 1 Diagnostic 4 2 Diagnostic 2 3 Diagnostic 1 4 Not used 5 Monitor Mode 4 6 Monitor Mode 2 7 Monitor Mode 1 3 Gates the status of Monitor State Latches 1-8 to Bus In lines 7 through 0 respectively.

TABLE 3-2. TAG DECODE AND CONTROL BUS FUNCTIONS (CONT'D)

Tag No. & Name	Notes and Function
12 (Cont'd)	BOB 4 Gates Check Status bits as follows: BIB0 CE Program Stop - Switch on unit tester set to Check Status 1 Motor On 2 Hds. Not Loaded 3 Even Cyl. 4 Interface Check 5 Monitor Check - set by Monitor Error 6 Interlocks not complete 7 Command reject 5 Gates fault byte bits to the bus in, as follows: BIB0 Data Fault,indicating a Select Lock condition 1 Servo Fault,indicating a power conflict condition 2 Write Overrun 3 Negative Voltage Fault 4 Positive Voltage Fault 5 Air Flow Fault 6 Multiple Hd. Fault 7 Current Fault 6 Test Logic. This bit is used to check the Device Check and Tag Valid circuits. Command Valid, consisting of Valid Command decode, Tag Active and Tag Decode Odd, must be active to perform the Test Logic function. Test Logic then forces a Tag Valid and turns on the Device Check latch.
13 Mode/Diagnostic Control	1. Unit must be selected. 2. Sets the following latches according to active bus out lines: BOB0 (Not used) 1 Diagnostic Mode 4 2 Diagnostic Mode 2 3 Diagnostic Mode 1 4 Block Parity 5 Monitor Mode 4 6 Monitor Mode 2 7 Monitor Mode 1 3. Gates the status of the Operating mode latches and the Diagnostic mode latches to the Bus In as follows: BIB0 Not used 1 Diagnostic Mode 4 2 Diagnostic Mode 2 3 Diagnostic Mode 1 4 Not used 5 Monitor Mode 4 6 Monitor Mode 2 7 Monitor Mode 1

Two logic circuits are used to control the seek function:

1. The Servo Circuit, which controls the voice coil positioner.

2. The Track Servo Circuit, which generates signals relating to the position of the heads over the disk pack. Its output is also used to generate the basic internal 806 kHz clock.

The general concepts of these two circuits are explained to provide the general background information needed to understand the specific types of seeks. Then more detailed explanations are provided for the three types of seeks: First Seek, Direct Seek, and Return to Zero Seek.

Although the machine clock, index, and sector detection circuits are not directly involved with Seek operations, their basic enable is provided by the signals generated by the Track Servo Circuit. These functions are, therefore, explained following the discussion on Seek operations.

SERVO CIRCUIT

The servo circuit is a closed loop servomechanism used to position the read/write heads. Figure 3-16 is a simplified schematic of the servo circuit. Functions of the major elements of the system are explained in Table 3-3.

A servo loop sums all of the error voltages imposed on it. The loop always attempts to maintain itself at a null. If not nulled, the loop will adjust the correctable device (in this case, the voice coil positioner) to achieve this null. Signals applied to the loop are called error voltages. Two major error voltages are used:

1. A position error: this is the departure of the positioner from the desired position.

2. A feedback signal to modify (or oppose) the position error to cause a smooth motion of the positioner.

TABLE 3-3. SERVO CIRCUIT FUNCTIONS

Circuit Element	Function
Difference Counter	Holds the complement of the number of tracks yet to be crossed before reaching the desired track or cylinder. Counter value is decimal 1023 (difference of zero) when on cylinder. An associated decoding network provides outputs representative of the current general content of the counter. In an Offset operation, the difference counter receives and holds offset distance information.
Digital to Analog Converter	Monitors the seven lowest order bits of difference counter to provide an analog indication of Position Error during the last 127 tracks (except last track) of all Seek operations.
Position Converter	Provides coarse Position Error signal, the amplitude of which is proportional to the number of tracks to go. Amplitude decreases in discrete steps (controlled by D/A converter) as last 127 tracks of a seek are crossed. Signal is inverted for reverse seeks.
Desired Velocity Function Generator	Processes Position Error signal at gain levels that vary as position Error decreases. The resulting output is the analog representation of the desired velocity curve to achieve maximum control of deceleration. The parallel non-linear feedback circuit maintains tight loop control by increasing gain as the Position Error signal approaches zero. This gain control prevents loss of control during the critical deceleration portion of the seek and is essential to minimize overshoot and settle out problems.

TABLE 3-3. SERVO CIRCUIT FUNCTIONS (CONT'D)

Circuit Element	Functions
Summing Amplifier	Generates a control signal to drive the power amplifier. Control signal based on algebraic summation of Position Error and Velocity Amplifier signal causes power amplifier to accelerate carriage. When Velocity signal exceeds Position Error, carriage decelerates.
Load Gate	Provides a constant positive input to the summing amplifier. This causes forward velocity of 7 ips.
RTZ Gate	Provides a constant negative input to the summing amplifier. This causes reverse velocity of 7 ips.
Power Amplifier	Responds to summing amplifier derived control signal to drive carriage mounted voice coil positioner. Current feedback is used to stabilize the gain of the power amplifier.
Velocity Amplifier	Amplifies signal of carriage mounted linear velocity transducer to provide an indication of velocity to the servo circuit. The associated amplifier disable forces amplifier gain to zero during a Power Off sequence (unload heads). This is required so that coupling between the positioner field and the velocity transducer does not cause oscillation during movement to the retracted position.
Velocity Integrator	Provides an integrated representation of velocity between each of the last 127 track pulses of a seek. Integrator is clamped off to gain of zero at all other times. Integrator output is a sawtooth waveform applied to input of desired velocity function generator between each track pulse to fill in or smooth out the stepped signal of the D/A converter (received via the position converter).
Fine Enable and Fine FF	Fine enable monitors integrated velocity. When difference counter is 1022 (T=1) and fine enable (Velocity integrator output) exceeds 1.28v, it indicates that there is one-half track to go. Fine FF sets to enable fine gate and clear coarse gate. This switches Position Error input to summing amplifier from desired velocity (coarse gate) to fine servo (fine gate). Fine also has the following effects: a. Turn on integrator clamp to switch off velocity integrator. b. Enables on cylinder detection. During load or RTZ sequences, both the fine and coarse latches are cleared. This disables both the fine and coarse gates so that motion is under control of load gate or RTZ gate.
Bit 0 Address Register and Odd Cyl FF	Used to select proper track servo signal phase for use as Fine Servo signal (signal controlling servo loop as last track is approached and carriage is stopped). If bit 0 is not set, the seek destination is an even numbered track and the track servo signal will be inverted for use in stopping the carriage. If bit 0 is set, an odd track is identified and track servo is not inverted. Register bit content is placed in Odd Cyl FF which performs actual gating.

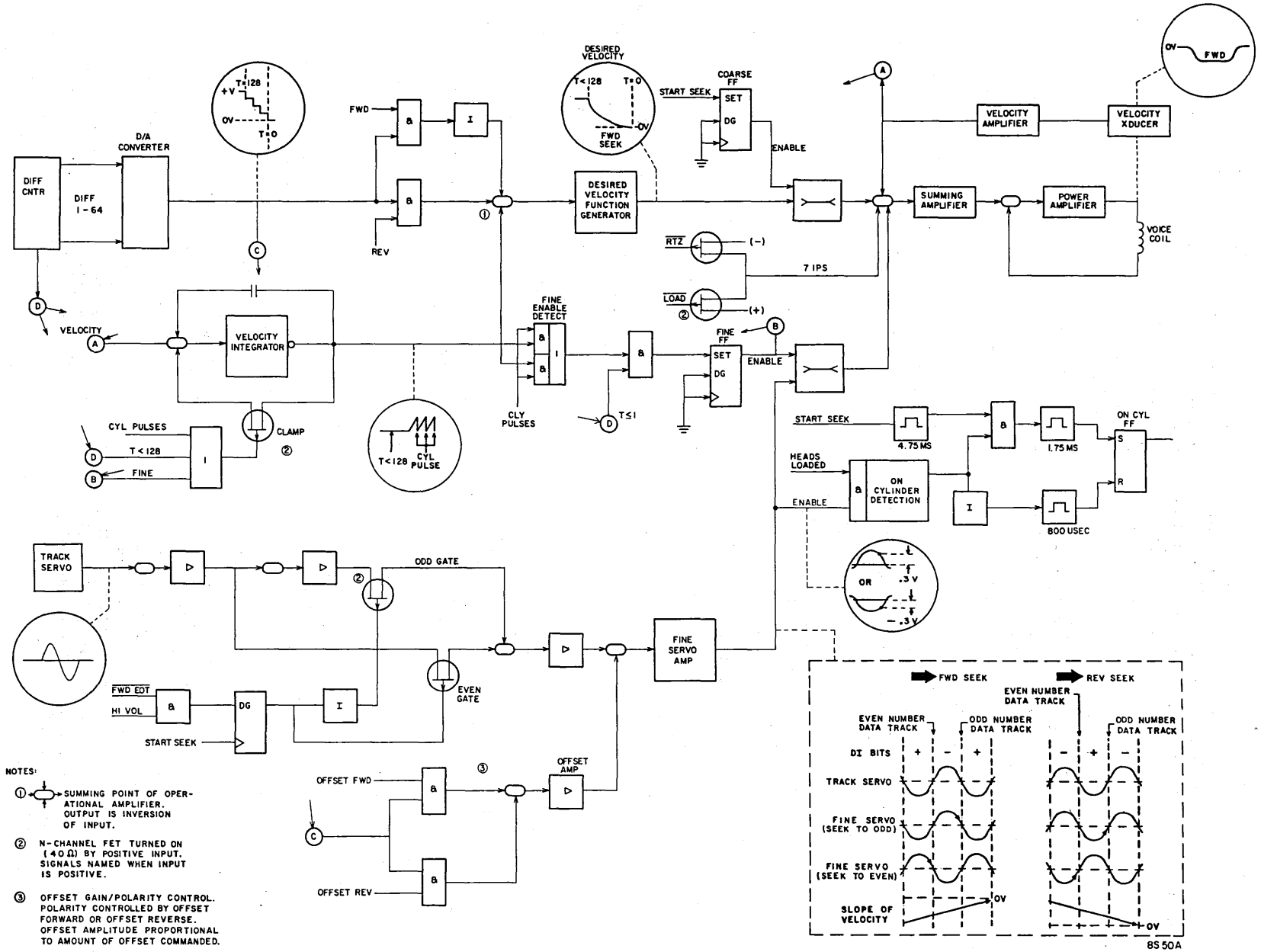
TABLE 3-3. SERVO CIRCUIT FUNCTIONS (CONT'D)

Circuit Element	Function
Fine Servo Amplifier	Provides the Fine Servo signal to the On Cylinder Detector and to the fine position amplifier. This signal amplitude is proportional to distance that heads are displaced from track centerline. Scale factor is one millivolt per microinch displacement. If heads drift off slightly after seek is completed, track servo signal is no longer null. This becomes fine servo signal to drive heads back into position. Carriage may be offset 25 to 775 microinches (in increments of 25 microinches) from nominal track centerline by application of offset voltage to fine servo amplifier. The voltage level is determined by Tag 8 Bits 3 through 7 when Offset Start (Tag 9 Bit 2) is received from the controller. Provides the Position Error signal, via the fine gate, to the summing amplifier during the last one-half track of the seek. Amplitude of this signal is proportional to distance-to-go. Phase is selected by Odd Cyl FF to be opposite in phase to velocity signal. The combination of the position error and velocity signals controls voice coil current to bring positioner into On Cylinder position.
On Cylinder Detector	Monitors fine servo signal when T≤1. When signal is less than about 0.3v, heads are close enough to track centerline to be assumed to be on cylinder. After 1.75 ms delay, On Cylinder is generated. If heads overshoot at end of seek so that voltage exceeds 0.7v, delay is reinitiated. Delay permits carriage to settle out before controller may attempt any read/write operations. The On Cylinder Detector is inhibited from triggering for 4.75 ms from the initiation of a Seek Start.

The position error signal is provided by the position converter and its allied elements. The amplitude of the signal is proportional to the distance from the present position to the desired position (tracks-to-go). The major feedback signal is the output of the velocity transducer. The amplitude of this signal is proportional to the velocity of the positioner while the phase indicates the direction of motion, forward or reverse.

The loop applies its position and feedback signals to one summing point, the summing amplifier. If the summation of these signals is not equal to zero, the summing amplifier outputs a signal proportional to the amplitude of the error voltage (which signifies the amount of displacement from the desired position) and the phase of the error voltage (which indicates the direction of displacement).

The error output from the summing amplifier is applied to the actuator assembly. The actuator contains a voice coil positioner that supports and moves the read/write heads. In turn, the voice coil is located within a powerful magnet. Whenever a current passes through the voice coil windings, the interaction of the induced emf and the magnet's flux field cause the positioner to move. The acceleration of the motion is proportional to the polarity and amplitude of the voice coil current.



NOTES:

① SUMMING POINT OF OPERATIONAL AMPLIFIER. OUTPUT IS INVERSION OF INPUT.

② N-CHANNEL FET TURNED ON (40 Ω) BY POSITIVE INPUT. SIGNALS NAMED WHEN INPUT IS POSITIVE.

③ OFFSET GAIN/POLARITY CONTROL. POLARITY CONTROLLED BY OFFSET FORWARD OR OFFSET REVERSE. OFFSET AMPLITUDE PROPORTIONAL TO AMOUNT OF OFFSET COMMANDED.

Figure 3-16. Servo Circuit Simplified Schematic

Basic Seek Operation

Seek operations are initiated by a series of control signals from the controller or by internally-generated signals within the drive during power up conditions. Most long seeks may be divided into four phases (see Figure 3-17):

1. Accelerate Phase: the voice coil receives full current to move the positioner from the current cylinder towards the new cylinder.

2. Coast Phase: velocity is at its maximum and the positioner velocity is constant.

3. Deceleration Phase: the positioner is approaching the desired cylinder. Its velocity must be reduced by braking action to prevent overshoot.

4. Stop Phase: the positioner is almost at the desired cylinder. It must be stopped at the precise centerline of the new data cylinder. The logic is in Fine mode to stop and hold the positioner at the new cylinder.

Refer to the various seek descriptions for detailed information on the exact seek sequencing.

Accelerate Phase

This phase is controlled largely by the position error signal. The controller loads the difference counter with the complement of the seek length. For example, if the heads are presently on cylinder 10 and must go to cylinder 160, the seek length is 150 cylinders. In binary representation, decimal 150 is 00 1001 0110. The complement of this number is 11 0110 1001, or decimal 873. At each cylinder pulse, the counter is incremented; therefore, the greater the number in the difference counter, the fewer tracks-to-go. The counter is at its maximum value of 1023 (11 1111 1111) when tracks to go equal zero.

The five low-order bits of the difference counter are applied to the position converter. The value of these bits indicates the position error (or tracks-to-go) from 0 to 127. That is, the amplitude of the position converter output is directly proportional to the number of tracks remaining in the seek. If the remaining seek length is greater than 127 ($T \geq 128$), the position converter output is clamped at its maximum saturated value to cause a very large position error.

The input to the summing amplifier is now a large signal. Since there is no velocity yet, the current through the voice coil is maximum, causing maximum acceleration. As the positioner accelerates, a velocity signal is generated by the velocity transducer. This signal opposes the position error signal. Its amplitude, however, is less. Acceleration continues.

Coast Phase

Eventually, the amplitude of the position error signal and the velocity feedback signal are equal. The net error signal in the loop drops to zero. The summing amplifier output follows, so current is cut off. Velocity is constant. Friction losses will tend to slow the positioner but, as it does, the velocity signal decreases. This allows the position error signal to call for more current.

Decelerate Phase

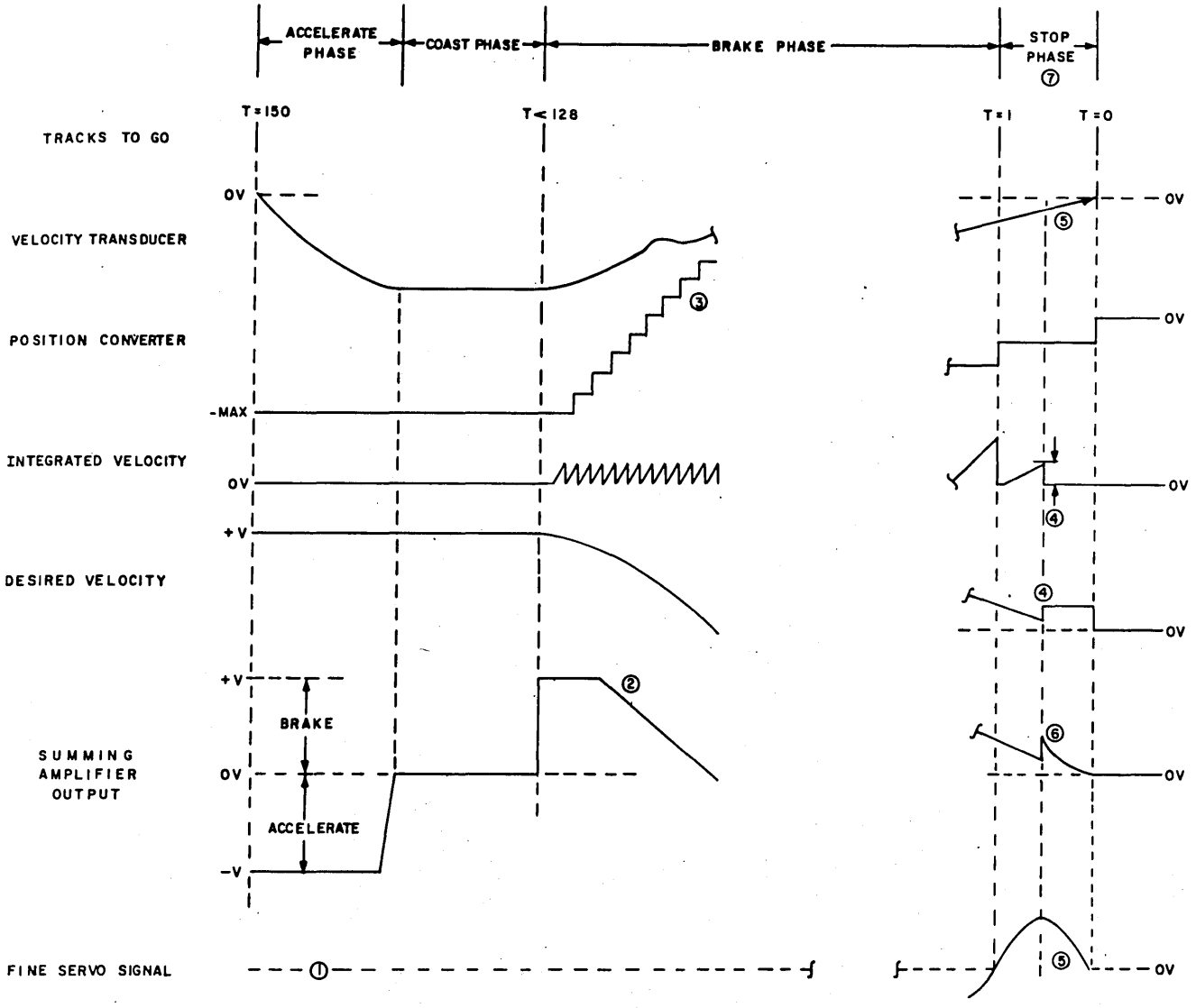
Braking action starts as the positioner approaches its selected cylinder.

The track servo circuit (refer to Track Servo Circuit description) has been generating cylinder pulses as each cylinder is passed. These pulses are used to increment the difference counter. When T=64, the position error signal from the desired velocity function generator is reduced. This causes the velocity signal to dominate and, since it is opposite in phase to the position error, the summing amplifier output switches polarity. Opposing current passes through the voice coil. The carriage decelerates. Both the desired velocity and velocity signals are decreasing simultaneously. Voice coil current decreases proportionately.

The loop maintains speed along an ideal velocity curve. This curve is the analog version of the number of tracks-to-go. The velocity curve is generated by the desired velocity function generator. Its output is compared with velocity to achieve maximum deceleration under all conditions without overshoot. The position signal is the sum of the following:

1. The position error signal from the position converter. Its output is a signal whose amplitude is proportional to the number of tracks-to-go.

2. Integrated velocity from the velocity integrator. Integrating a velocity signal provides a signal



NOTES:

① SIGNAL HAS NO EFFECT UNTIL FINE LATCH SETS.

② SLOPE DETERMINED BY LOOP GAINS TO PERMIT SERVO CONTROL ALONG DESIRED CURVE.

③ OUTPUT DECREASES WITH EACH CYLINDER PULSE.

④ FINE LATCH SETS WHEN T ≤ 1 AND INTEGRATED VELOCITY > 1.28V. DESIRED VELOCITY HAS NO FURTHER EFFECT.

⑤ COMBINATION OF THESE TWO SIGNALS CONTROLS OUTPUT FROM SUMMING AMPLIFIER.

⑥ GAIN CHANGE CAUSED BY SWITCH FROM COARSE TO FINE CONTROL. ALTHOUGH CONTINUOUS BRAKING ACTION IS ILLUSTRATED, OUTPUT MAY BE NEGATIVE (ACCELERATE) IF FINE SERVO SIGNAL EXCEEDS VELOCITY SIGNAL.

⑦ SCALE CHANGED AT T=1 FOR CLARITY.

8. DRAWING NOT TO SCALE FOR TIMING OR RELATIVE SIGNAL AMPLITUDE. IT IS SIMPLIFIED TO ILLUSTRATE SIGNAL FUNCTIONS.

8W30

Figure 3-17. Servo Circuit Simplified Signals

proportional to distance. This signal is a sawtooth waveform: it is pulled back to zero by each cylinder pulse and increases in proportion to velocity and time (distance). The combination of the stepping-down output from the position converter with the ramp integrated velocity signal results in a smooth curve of constantly-decreasing magnitude.

3. The function provided by the nonlinear feedback around the desired velocity function generator.

Stop Phase

Stop Phase begins when the difference counter indicates that there is one track-to-go. When T=1, the velocity integrator signal is pulled back to zero by the cylinder pulse. Its output, indicating distance, increases. When its amplitude indicates approximately one-half track remains, Fine Enable sets the Fine latch. Desired velocity is disabled since the coarse latch is opened by Fine being set.

The last half-track of motion is controlled by the fine servo signal. There is a significant increase in position error gain in switching from coarse to fine. Fine servo and velocity are applied to the summing amplifier. The summation of these two signals control the braking current.

At the start of the seek, the Odd Cylinder FF is set if the seek is to an odd-numbered cylinder. The odd cylinder signal controls the phase of the track servo signal applied to the fine servo amplifier. This adjustment is required since track servo signal phasing is a function of the servo head position: the signal is negative when over negative dibits and positive when over positive dibits. Therefore, on forward seeks, the signal is decreasing from a negative value toward zero when approaching a data track with an odd number; it is increasing from a positive value toward zero when approaching a data track with an even number. The opposite is true during a reverse seek.

Phasing of the track servo signal is selected so that the fine servo signal opposes the velocity signal during the last half-track of the seek. Both signals are decreasing. If either is greater, the summing amplifier makes minor braking current adjustments. When the heads are on cylinder, both signals are zero and current is zero.

When the fine servo signal is less than about 0.3v, the positioner is, for all practical purposes, positioned over the data track. If the 4.75 ms delay initiated at the start of the seek has timed out, the 1.75 ms On Cylinder Delay is initiated. After 1.75 ms, On Cylinder is generated.

The fine servo signal remains active even through On Cylinder is up. This is the track following or position error operation. Since the positioner is not mechanically locked in place, it can drift off cylinder. As long as it is precisely positioned, the dibits read from the adjacent dibit tracks are equal and opposite. Should the carriage move,one dibit signal will increase in amplitude. This results in a slight track servo signal which is translated into the fine servo signal. The summing amplifier, in turn, senses this off-null condition and drives the positioner back on cylinder.

If the positioner goes off cylinder sufficiently to cause the fine servo signal greater than 0.7v for more than 800 μsec, the On Cylinder signal is lost. This sets Seek Incomplete, and deselects the heads. If the unit is reading or writing at the time Select Lock and Device Check are also set.

Offset Head Positioning

Besides the normal seek operations, the servo circuit positions the heads during an Offset operation. The heads are held off the track centerline by an amount and direction determined by a Transmit Offset command (Tag 8, Bit 0 determines direction of offset. Bits 3-7 determine amount of offset). Heads must be On Cylinder and an Offset Start command (Tag 9,Bit 2) must be received before the Transmit Offset will be acted on. In the offset mode, the output of the difference counter is steady and proportional to the amount of offset desired. This raises the fine servo signal to the fine position amplifier and causes the heads to be driven off track centerline until the servo loop achieves a null. Direction of offset is determined by the polarity of the Fine Servo signal. The Offset Active signal (Tag 11 - B1) is set high by Offset Start and remains high until disabled from the controller by Offset Reset (Tag 10-B7).

Short Seeks

The preceding explanation of the basic seek operation presumed long seeks that permitted the positioner to attain maximum velocity.

Maximum velocity of about 60 ips requires 70 tracks acceleration time. During short seeks, gating is identical although relative phasing of the error signals will vary. During seeks less than 128 tracks, certain signals are available immediately: integrated velocity, non-linear feedback to the desired velocity function generator, and a position converter output not clamped at its maximum value. These signals generate a position error voltage to accelerate the positioner.

The voice coil saturates for a shorter time but the primary function remains unchanged: acceleration occurs when the position error signal exceeds the velocity signal; braking occurs when the velocity signal exceeds the position error signal.

TRACK SERVO CIRCUIT

Basic Description

The track servo circuit provides head positioning information. The signals generated by this circuit:

1. Generate a track servo signal that indicates the displacement of the heads from their nominal track centerline.
2. Generate indications that the heads are positioned outside of the normal data cylinders.
3. Generate cylinder pulses during seeks to indicate each cylinder crossing.
4. Provides signals used as the basic 806 kHz clock.

Information for this circuit is derived from the track servo head (Figure 3-18). This head is physically similar to the read/write heads, except that it does not write. The head reads information from the servo track surface of the disk pack. This information is known as dibits: dibit is a shortened term for dipole bit. Dibits are prerecorded on the servo surface during manufacture of the disk pack. Do not confuse the servo surface with the other 19 disk pack recording surfaces.

Dibits are the result of the manner in which flux reversals are recorded on the servo tracks. One type of track, known as the Even track, contains negative dibits. The other track, the Odd track, contains positive dibits.

There are 883 dibit tracks on the servo surface. At the outer edge of the surface is a band of 24 positive dibit tracks. This area is the Reverse End of Travel (EOT) or outer guard band. Then, there are 823 servo tracks alternately recorded with negative and positive dibits. Finally, toward the inner edge of the pack, there are 36 tracks containing only negative dibits. This is the Forward EOT or inner guard band.

When the read/write heads are located at the centerline of a data track, the track servo head is actually centered between two of the prerecorded servo tracks and is reading an edge of each. The detected signal is a mixture of the two adjacent dibit signals. The amplitude of each dibit component is proportional to the read coil overlap of the recorded servo tracks. With the head centered, the amplitudes of the two types of dibits are equal. As the head moves away from its centered position, the amplitude of one dibit component increases while the other decreases. This error voltage is the track servo signal.

Circuit Description

The basic elements of the track servo circuit are illustrated in Figure 3-19. Table 3-4 explains the track servo circuit functions.

Dibit Gating

After being differentially amplified, the servo signal is applied to gates that separate the dibit signals by sensing the positive and negative flux reversals (Figure 3-20). A positive dibit consists of a positive-going waveform immediately followed by a negative-going waveform. On the other hand, a negative dibit consists of a negative-going waveform followed immediately by a positive-going waveform.

The dibits are analyzed by the positive and negative gates. Each gate output switches to the low state when it senses its respective dibit. The negative-going pulses control single-shots and JK FF's to generate the odd/even dibits.

The even/odd dibits are used to enable the EOT detection circuit and to generate the basic machine clock signal.

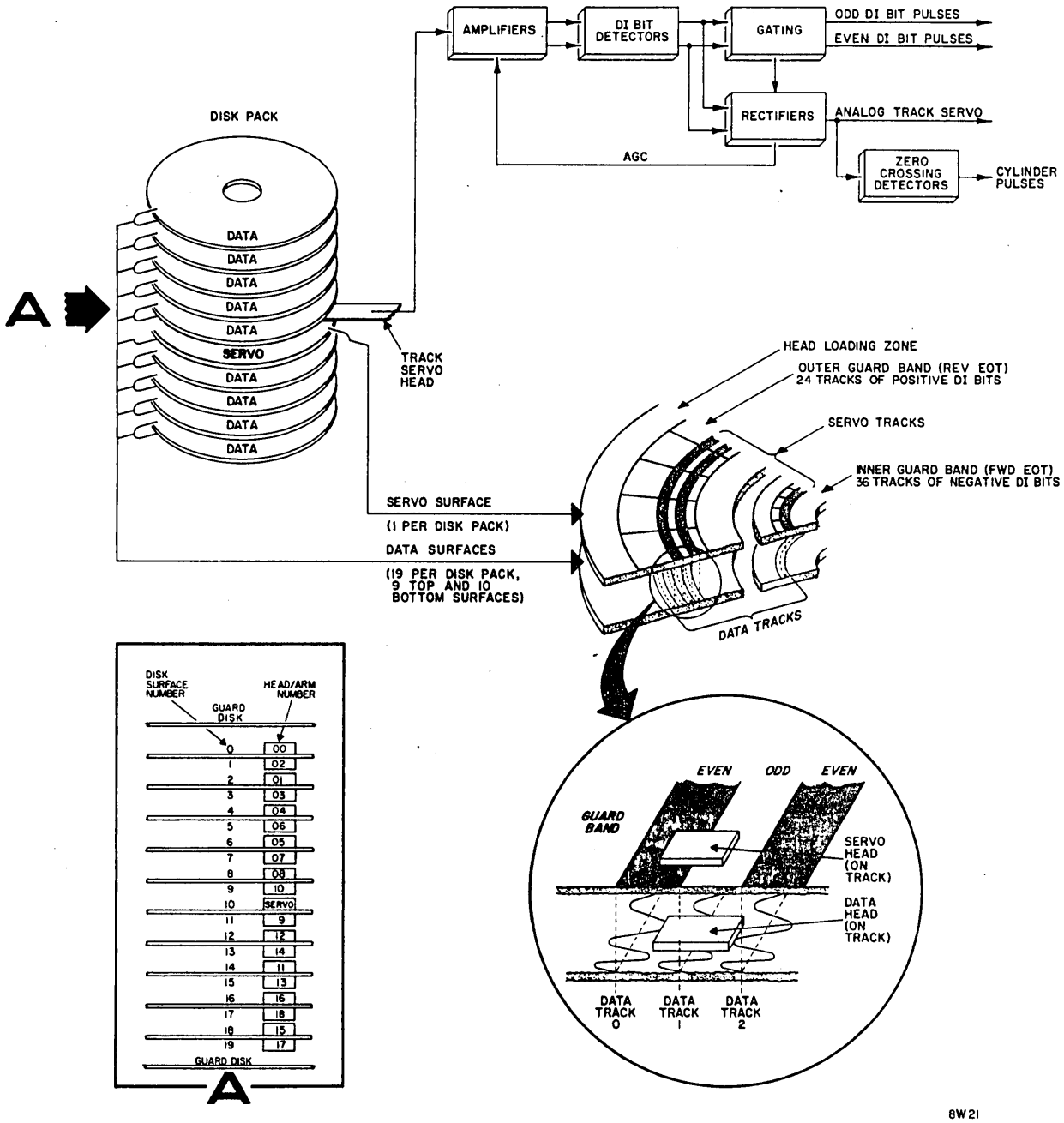


Figure 3-18. Track Servo Disk Layout

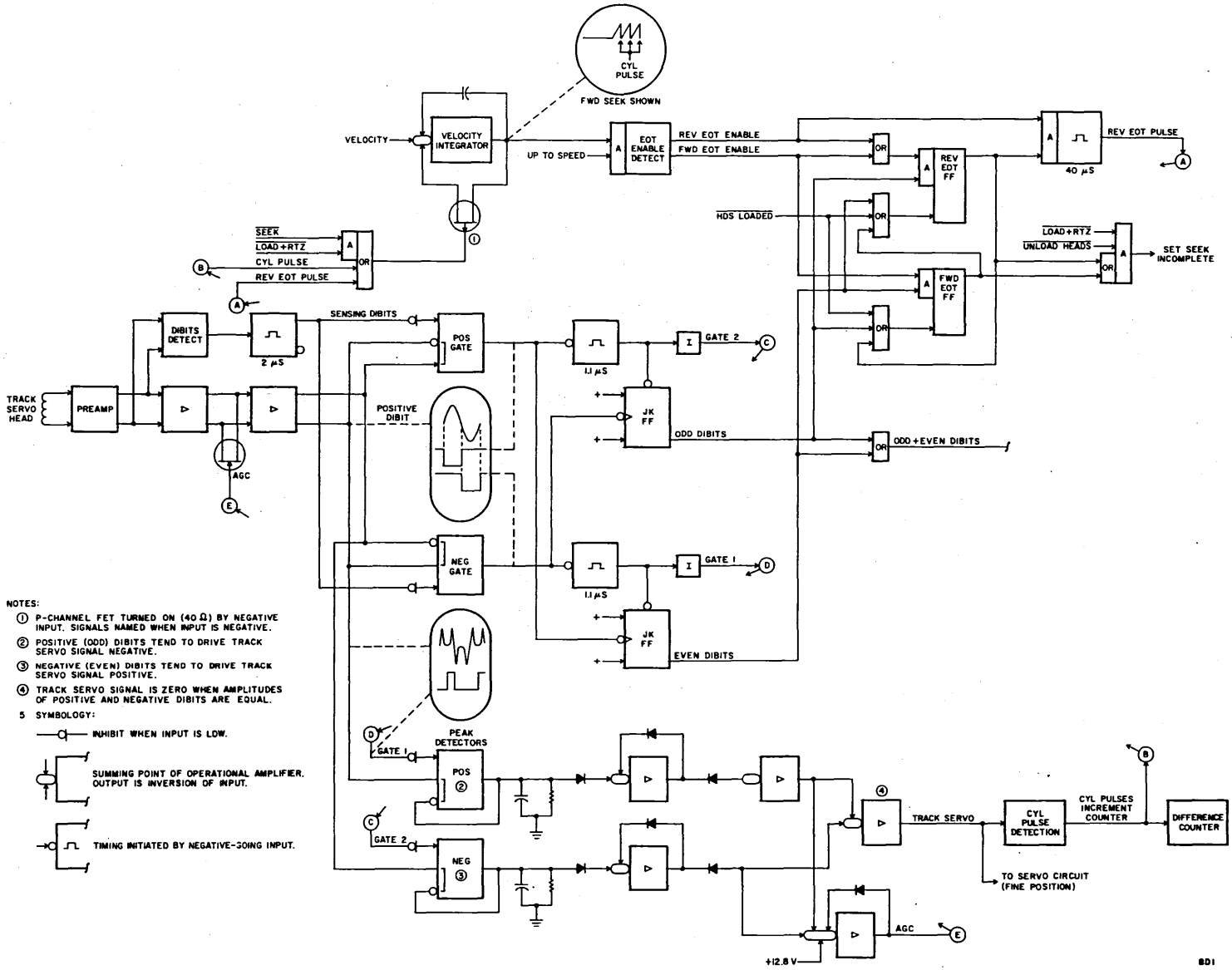


Figure 3-19. Track Servo Circuit Simplified Schematic

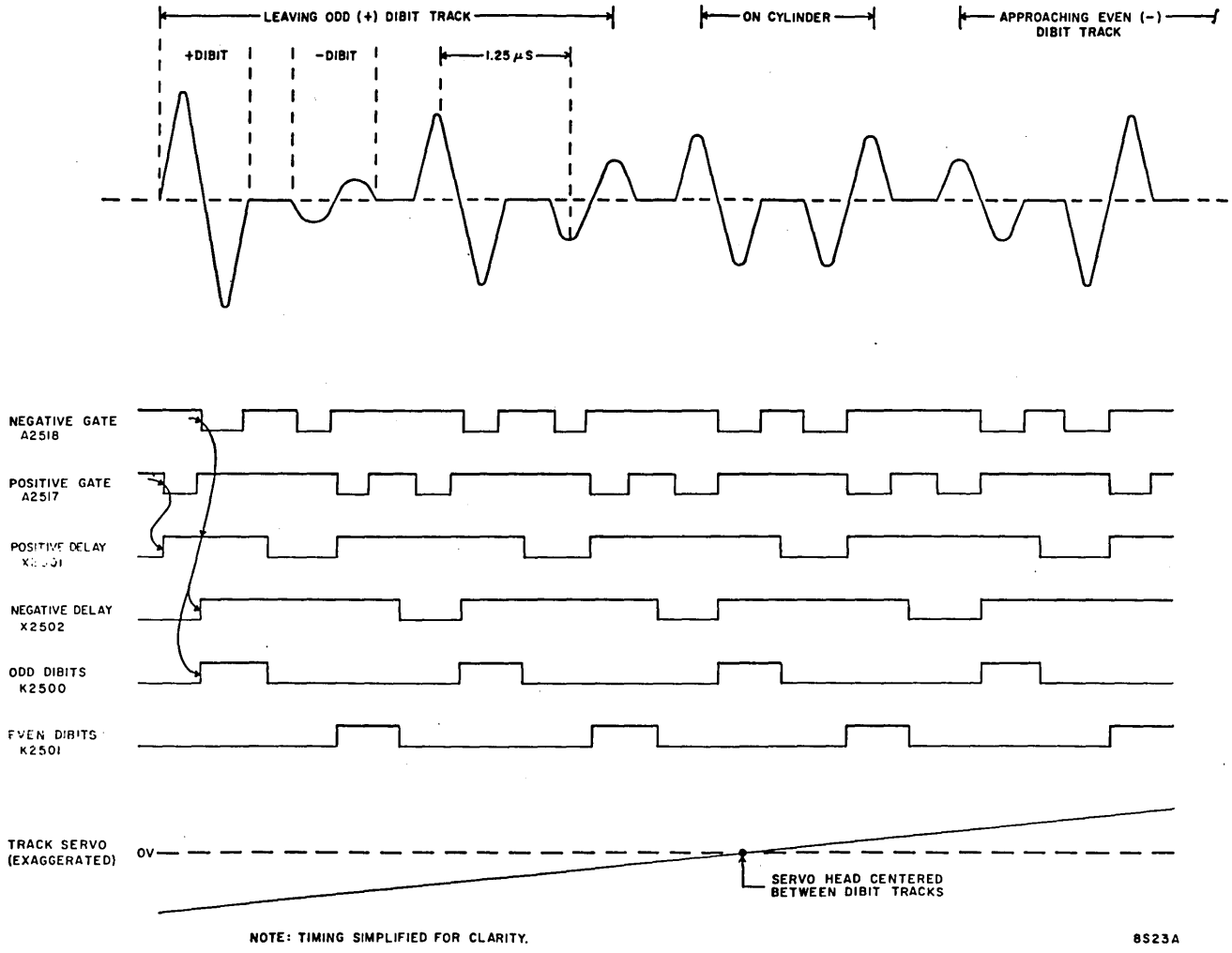


Figure 3-20. Track Servo and Dibits Detect Circuit Simplified Signals

TABLE 3-4. TRACK SERVO CIRCUIT FUNCTIONS

Circuit Element	Function
Track Servo Head	Reads dibit information from the disk servo tracks. This head cannot write.
Track Servo Preamplifier	Amplifies the signal read by the track servo head.
Positive and Negative Gates	Separate dibit waveforms into positive and negative components. Positive gate triggers during first half-cycle of positive dibits (read from odd dibit track) and second half-cycle of negative dibits (read from even dibit track). Negative gate triggers in the reverse condition.
Positive and Negative Delays	Function as synchronizing gates to control dibit pulses generation. Positive delay fires at leading edge of positive gate. If negative gate output is available before positive delay times out, it indicates that positive dibit has been sensed. This triggers the Odd Dibit FF. The positive gate also serves as an inhibit to the positive peak detector during the negative portion of the positive dibit and the entire negative dibit. The negative delay functions in the reverse condition.
Even Dibits and Odd Dibits Flip-Flops	Provides 600-nsec pulses indicating dibits. Frequency of each one-shot is 403 kHz.
Dibits Peak Detectors	Provide peak detection of dibit signals. Outputs are proportional to dibits amplifiers: the greater the amplitude, the more negative the output. When head is centered between dibit tracks, outputs of + and - peak detector are equal. As head moves from center position, output from one peak detector increases negatively while output from the other peak detector becomes less negative. The difference between these two outputs is proportional to servo head displacement from centered (on cylinder) position.
AGC Circuit	AGC voltage is proportional to sum of dibit signals. As signal strength increases, voltage goes less negative to reduce circuit gain.
Track Servo Amplifier	Provides signal proportional to sum of + and - dibit peak detectors. Output is null when head is centered between dibit tracks (on cylinder); negative when over odd track or outer guard band; positive when over even track or inner guard band.
Cylinder Pulse Detection	Provides cylinder pulses to difference counter and other logic elements as track servo signal approaches null. One pulse is generated per track crossed (even/odd transition or odd/even transition).
Velocity Integrator	Provides ramp signal proportional to distance travelled (velocity integrated with time). Output is positive-going during forward seek; negative-going during reverse seek. Output is pulled back to zero to re-initiate integrator function by each cylinder pulse, or during certain conditions of RTZ or Load sequences.

TABLE 3-4. TRACK SERVO CIRCUIT FUNCTIONS (CONT'D)

Circuit Element	Function
Dibits Detect	50 µsec and 3 ms delays used to prevent the track servo circuit from being turned on by random noise spikes during a heads unloaded condition or a load heads operation.
End of Travel (EOT)	Monitors integrated velocity to enable EOT circuit. When velocity integrator output exceeds about 1.2v, heads have moved a distance of approximately two tracks without sensing any cylinder pulses.
Reverse EOT FF	Indicates that heads are positioned over outer guard band. Refer to First Seek and RTZS discussions for further details.
Forward EOT FF	Indicates that heads are positioned over inner guard band. This is an error condition.

Track Servo Signal

The servo signal is generated by peak detectors that monitor their respective dibits. The positive peak detector (Figure 3-20) provides an output proportional to the amplitude of the positive dibits. It senses only the positive waveform of positive dibits: Gate 1 low inhibits it from reacting to either the negative waveform of positive dibits or the entire negative dibit. An RC network integrates the peak detector output to provide a smooth output. The resulting signal output is greatest, therefore, when the servo head is centered over an odd dibit track.

The negative gate works in a similar manner.

The servo signal is provided by a summing amplifier. It receives inputs from the peak detectors. (The positive peak detector output is first inverted.) Therefore, the output represents the difference between the two peak detector outputs.

The track servo signal is at its maximum negative value when the servo head is positioned over the outer guard band or over one of the odd dibit tracks. It is at its maximum positive value when the servo head is positioned over the inner guard band or over one of the even dibit tracks.

The track servo signal is applied to the servo circuit and to the cylinder detect circuit. In the servo circuit, it is used to generate the fine servo signal that controls movement during the last one-half track of a seek or during a Load sequence. The cylinder detect circuit generates cylinder pulses as the track servo signal approaches a null.

Circuit gain control is achieved by applying the outputs from the peak detector buffers to the AGC summing amplifier. Its output is negative in proportion to signal strength: the stronger the signal, the less negative the AGC voltage. This signal is fed back to the AGC amplifier to control the resistance of a FET within the amplifier. The FET is connected across the differential inputs to the amplifier. The less negative the AGC, the less the resistance; therefore, more of the signal from the track servo head is shunted by the FET to reduce circuit gain.

The Dibits Detect single shots (X2503 and X2500) prevent the circuit from being turned on by random noise spikes while the heads are unloaded or being loaded. When the preamp output is zero, as in a heads unloaded condition, X2503 is not triggered and its output is high. This holds X2500 at a logic zero. The positive and negative gates and cylinder detect circuits are now inhibited.

When the heads are loaded and dibits are outputed from the preamp, X2503 is triggered and retriggered, keeping its output at a logic zero. This releases the timing components of X2500 and after 3 ms its output goes to one turning on the Track Servo circuit. If dibits are lost for more than 50 µsec, X2503 times out and resets X2500 to a logic zero, disabling the Track Servo circuit (see Figure 3-21).

End of Travel Detection

The End of Travel (EOT) circuit determines when the heads are positioned outside of the normal data cylinders. This function is used during Load and RTZ sequences and to indicate an error condition during a seek.

Forward EOT indicates that the heads are within the inner guard band. Assume that the controller has commanded a forward seek to an illegal cylinder past cylinder 822. Sequencing is as follows (refer to Figure 3-19).

1. As the heads move forward, the velocity integrator output produces a signal proportional to velocity (the input to the integrator) and time (provided by the integrator capacitor). The output, which is a positive-going ramp during forward seeks, represents distance travelled. It is pulled back to ground by cylinder pulses. As long as cylinder pulses are generated, the output cannot reach an effective value.

2. After track 822 is passed, no more odd dibit tracks are detected, resulting in no more cylinder pulses to reset the velocity integrator. When the output exceeds approximately 1.25 volts (4-8 tracks), Forward EOT Enable comes up. This signal, in conjunction with the even dibits picked off of the inner guard band, sets the Forward EOT FF.

3. With the Forward EOT FF set:

   a. Seek FF (set at the start of the seek) is cleared. This stops the seek function. The output of the position converter in the servo circuit is blocked to indicate a zero position error.

   b. The difference counter is set to 1023 (T=0).

   c. Fine Enable is raised within the servo circuit.

   d. Because of b and c, the Fine FF in the servo circuit is enabled.

   e. The Odd Cylinder FF is cleared to indicate a seek to an even-numbered cylinder.

   f. Index counter is reset to zero and held there until the Forward EOT FF is cleared.

   g. EOT Seek Error FF sets resulting in steps h and i.

   h. A Seek Incomplete Signal (Tags 4 and 9, BIB2).

   i. The Seek Complete FF is held clear, preventing a Seek Complete signal until the EOT Seek Error FF is cleared.

4. The track servo, functioning as the fine servo signal in the servo circuit, is gated to the servo summing amplifier via the Fine FF. The signal is at a maximum amplitude

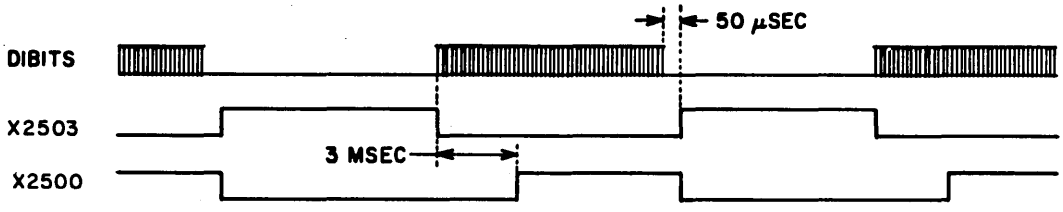


Figure 3-21. Dibits Detect

because only even dibits are being sensed. This error voltage causes the positioner to drive in reverse until the servo signal drops to zero: the heads are then positioned at cylinder 822. The EOT FF is cleared by the odd dibits.

5. The positioner has 500 ms after Forward EOT FF is set to generate On Cylinder at cylinder 822. If not, Seek Incomplete FF is set.

6. To clear the fault, the controller must issue a Rezero Start command (Tag 9, Bit 4).

Reverse EOT indicates that the heads are positioned over the outer guard band. If this condition occurs during regular reverse seeks, the Reverse EOT FF sets. This initiates an automatic Load sequence to return the actuator to cylinder 000. The same error condition exists, however, as if a Forward EOT occurred.

Cylinder Pulse Generation

As the servo head crosses the interface of the even/odd dibit tracks (Figure 3-22), the servo signal decreases toward null. Two operational amplifiers connected as Schmitt triggers switch state. The hysteresis designed into the circuit causes both triggers to be up only while the servo signal is between 0v and 0.4v. These signals are applied to two level shifters (A3002/A3003). Their outputs are ANDed together to provide a 10 microsecond cylinder pulse. Each cylinder pulse:

1. Increments the difference counter.

2. Switches the two velocity integrators (one each in the servo circuit and track servo circuit) to ground.

It is possible that the last cylinder pulse may not be generated when the seek is completed, causing the difference counter to hang up at 1022. The On Cylinder signal provides a pulse to increase the difference counter to 1023.

The track servo circuit remains active following completion of a seek. If the servo head drifts off of its centered position, the track servo signal will no longer be at null. The signal, functioning as the fine servo signal within the servo circuit, will act as a position error signal to drive the positioner back into position.

FIRST SEEK

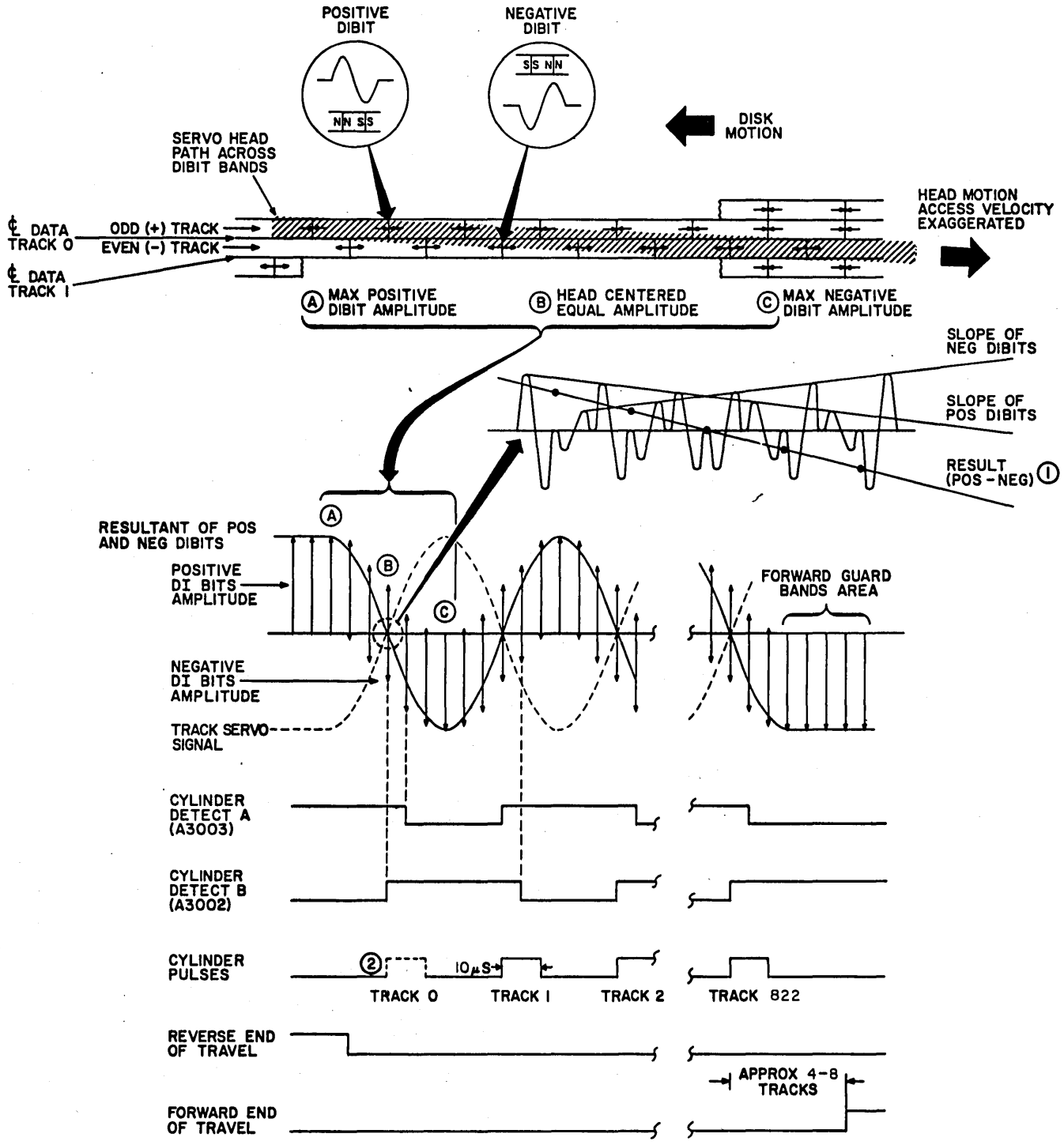
This function, also known as the Load sequence, involves the activities that a unit must perform before it can effectively respond to a Read, Write, or Seek command from the controller. This function consists mainly of power supply relay sequencing and status checking by the unit's logic. As a result, no actual selection of the unit is required and very little drive/controller signal exchange occurs. Successful progression of the function assumes that all circuit breakers are on, disk pack is installed on spindle of unit, and the interlocks are closed. Successful completion of a First Seek is signified by Seek Complete (Tag 4 and 9, BIB3) and On Line (Tag 4 and 9,BIB4) going high. Busy Status (Tag 4 and 9,BIB6) drops and the Physical Unit Identification indicator lights. During First Seek operation, Monitor Mode 4 FF is set.

As the operation continues, the State FFs associated with certain events are set, in order. If the State FF for an event is not set or the State FFs are set out of order, the Device Check FF is set. The Device Check signal requires only that the unit be selected to be received by the controller. No prior tag is necessary. The Device Check signal can only be cleared by a Control Reset (Tag 9, Bit 6) a Power On reset, or from the Operator panel or tester.

Initiation of the function occurs when the START switch is pressed (Figures 3-23 and 3-24). Refer to the power supply discussion in this section for additional sequencing information. Busy status is available. The logic enables motor relay K3. This causes release of the hysteresis brake and starts the spindle motor. At the same time, the first seek interlock motor is energized to initiate a first seek delay cycle.

When the disk pack speed reaches 3000 rpm, the power supply relay K2 energizes to apply +20v power to the read/write logic and to energize retract relay K5 (the heads are unloaded) to connect the positioner voice coil to the power amplifier driven by the servo logic.

At the end of the 15-second (approximate) cycle, the first seek interlock switch transfers and activates the first seek operation by setting the Load latch. The Load latch drives the Load gate; this bias voltage forces an average forward 7 ips access that mechanically loads the heads. The carriage continues forward with the servo head searching for the prerecorded positive dibits signals on the track servo surface.



NOTES: ① TRACK SERVO SIGNAL (A2503) IS 180° OUT-OF-PHASE WITH THIS WAVEFORM.
② CYL PULSE DOES NOT AFFECT DIFFERENCE COUNTER AT TRACK 0 FOR FIRST SEEK.

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Figure 3-22. Cylinder Pulses Generation

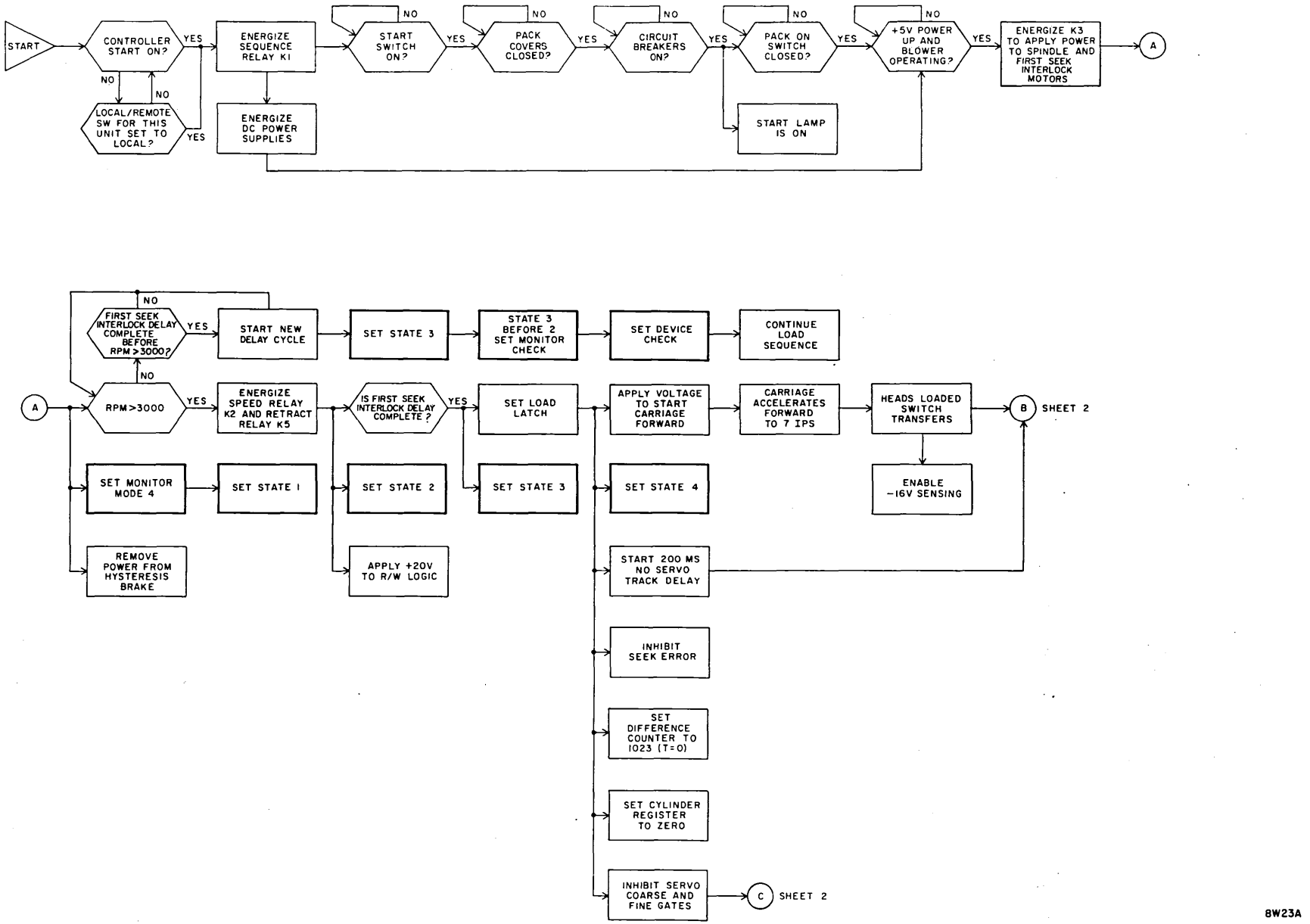


Figure 3-23. First Seek Flow Chart (Sheet 1 of 2)

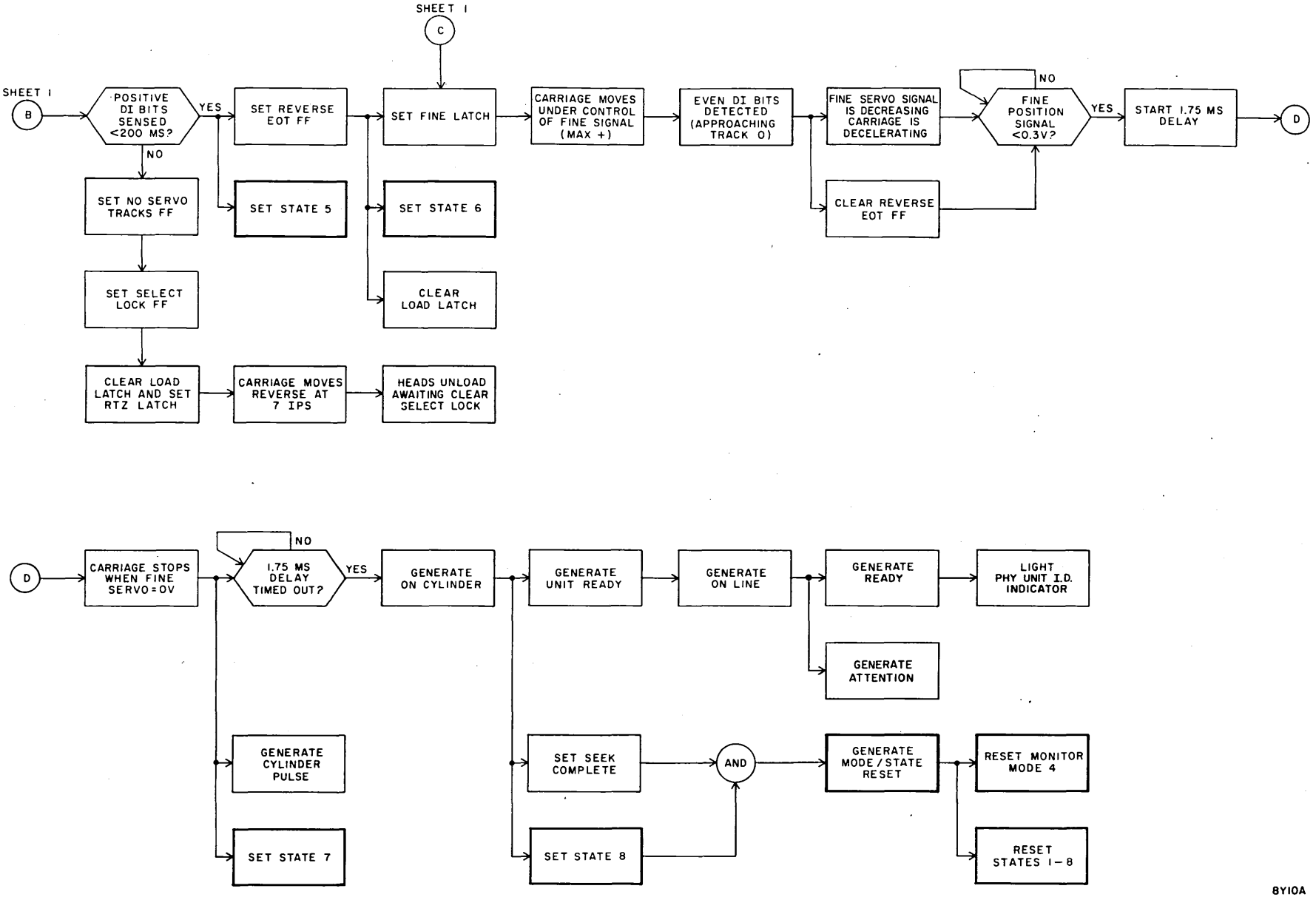
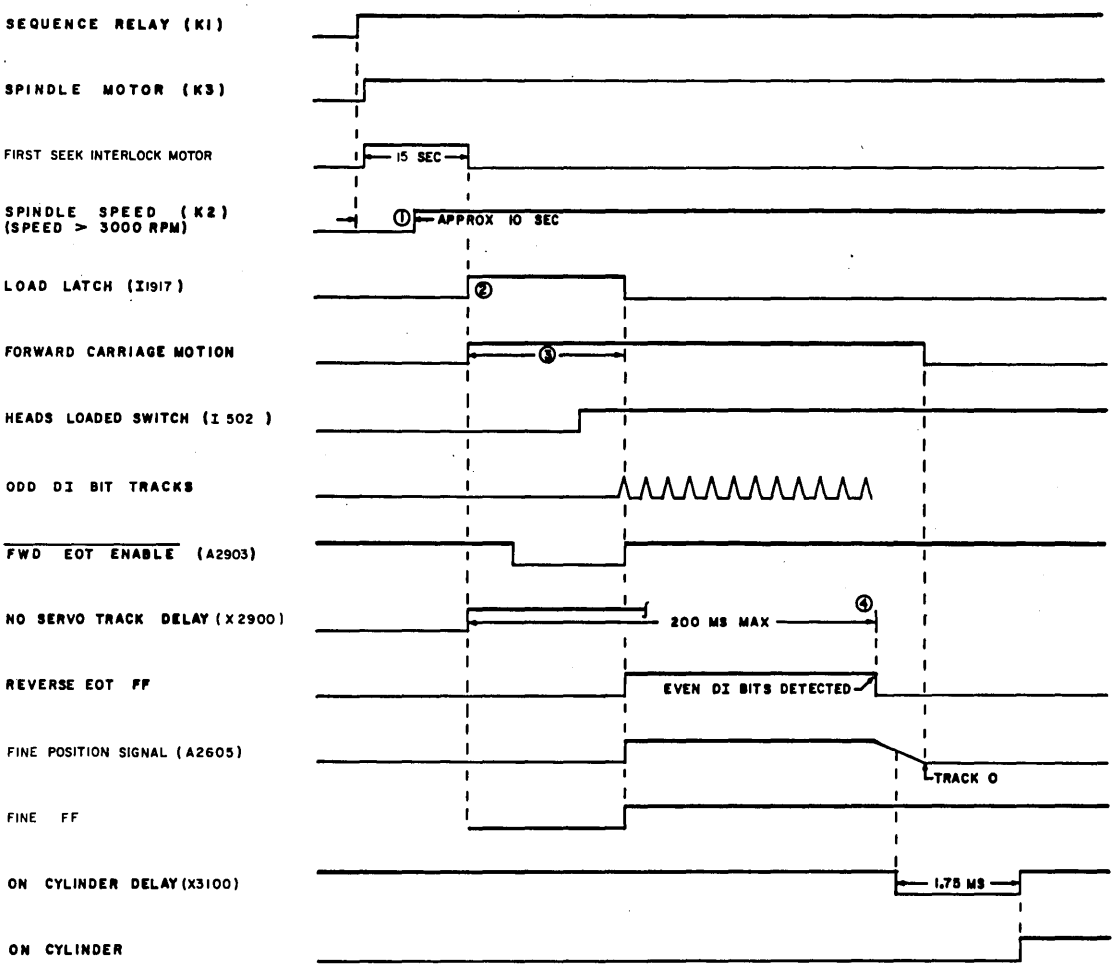


Figure 3-23. First Seek Flow Chart (Sheet 2 of 2)



NOTES:

① RETRACT RELAY K5 PICKED WHEN K2 PICKS.

② LOAD FF CAUSES LOAD GATE (A2903) TO APPLY + (SEEK FWD) VOLTAGE TO VOICE COIL SUMMING AMPL. COARSE AND FINE GATES INHIBITED. CYLINDER REGISTER SET TO ZERO AND DIFFERENCE COUNTER SET TO MAXIMUM (1023).

③ MOTION TO 7 IPS PROVIDED BY LOAD GATE UNTIL ODD DI BITS SET REVERSE EOT FF. MOTION CONTROL THEN PROVIDED BY FINE SERVO SIGNAL

④ DI BITS MUST BE DETECTED WITHIN 200 MS OR SELECT LOCK IS SET. HEADS UNLOAD. SELECT LOCK MUST BE CLEARED BEFORE ANOTHER LOAD ATTEMPT CAN BE MADE.

8W 298

Figure 3-24. First Seek Timing Diagram

When the Reverse EOT area (all odd, or positive, dibits) is sensed, the Load latch is cleared and the Fine gate is enabled. The carriage now servoes into cylinder 000 under control of the fine servo signal.

When the positioner reaches cylinder 000, On Cylinder is generated. After a 1.75 ms delay, the On Cylinder FF sets. This has the following effects:

1. Unit Ready FF sets. It can be cleared only when the heads unload.

2. The Attention FF is set by Unit Ready, assuming a Logical Address Plug is in place.

If, for any reason, the dibit signals are not detected by the track servo logic within 200 ms after the Load latch is set, the RTZ latch will be set. The positioner will retract to the heads unloaded position. In this case, a Pack Unsafe (Device Fault and SELECT LOCK indicator on) condition exists to prevent reloading until the Select Lock FF is cleared. The same conditions exist if the dibits are lost for 200 ms after Unit Ready is available. Refer to Seek Status and Error Conditions for other First Seek Errors.

DIRECT (FORWARD/REVERSE) SEEK

The Direct Seek function involves those operations that must be performed to move the read/write heads from their present track or cylinder location to the one specified by the controller.

The basic principles of the seek operation are explained in the Servo Circuit discussion.

I/O Sequencing

Controller/drive signal interchanges during a seek function from cylinder 10 to cylinder 160 would be as follows (see Figures 3-25 and 3-26).

NOTE

Except as specified below, the actual sequence may be varied without affecting drive operations. This is a typical sequence.

1. Controller issues a Transmit Cylinder Address Tag (Tag 6).

   a. Bits 0 and 2 of the tag are raised, transmitting a new cylinder address of 160_{10}.

   b. The new cylinder address is loaded into the Cylinder Address register.

   c. Reset Head Address register to zero.

   d. Reset difference counter to 1023.

2. Controller issues a Transmit Head Address Tag (Tag 7)

   a. The bits of this byte are:

BOB0	Cylinder Address
	Register 512
1	Cylinder Address Register 256
2	Not used
3	Head Address 16
4	Head Address 8
5	Head Address 4
6	Head Address 2
7	Head Address 1

   b. Because the seek will be forward, less than 256 tracks, and the head 10_{10}, the tag byte will be: 0000 1010.

   c. Bits 256 of Cylinder Address register and difference counter are loaded.

   d. The new head address is loaded into the Head Address register.

3. Controller issues a Transmit Difference Tag (Tag 8) and Transmit Control 2 (Tag 10, BOB2).

   a. The difference between present location and destination is 150_{10}. Therefore, 150_{10} is placed on the bus out to the drive.

   b. The complement of 150_{10} enters the lower eight bits of the difference counter. The contents of the difference counter is now 723_{10}. (See Figure 3-25).

4. Controller issues Seek Start command (Tag 9, BOB3).

5. Drive decodes the command and, as long as there is not a Fault, proceeds to execute the seek. The Seek Forward FF, Forward FF and Seek FF are set.

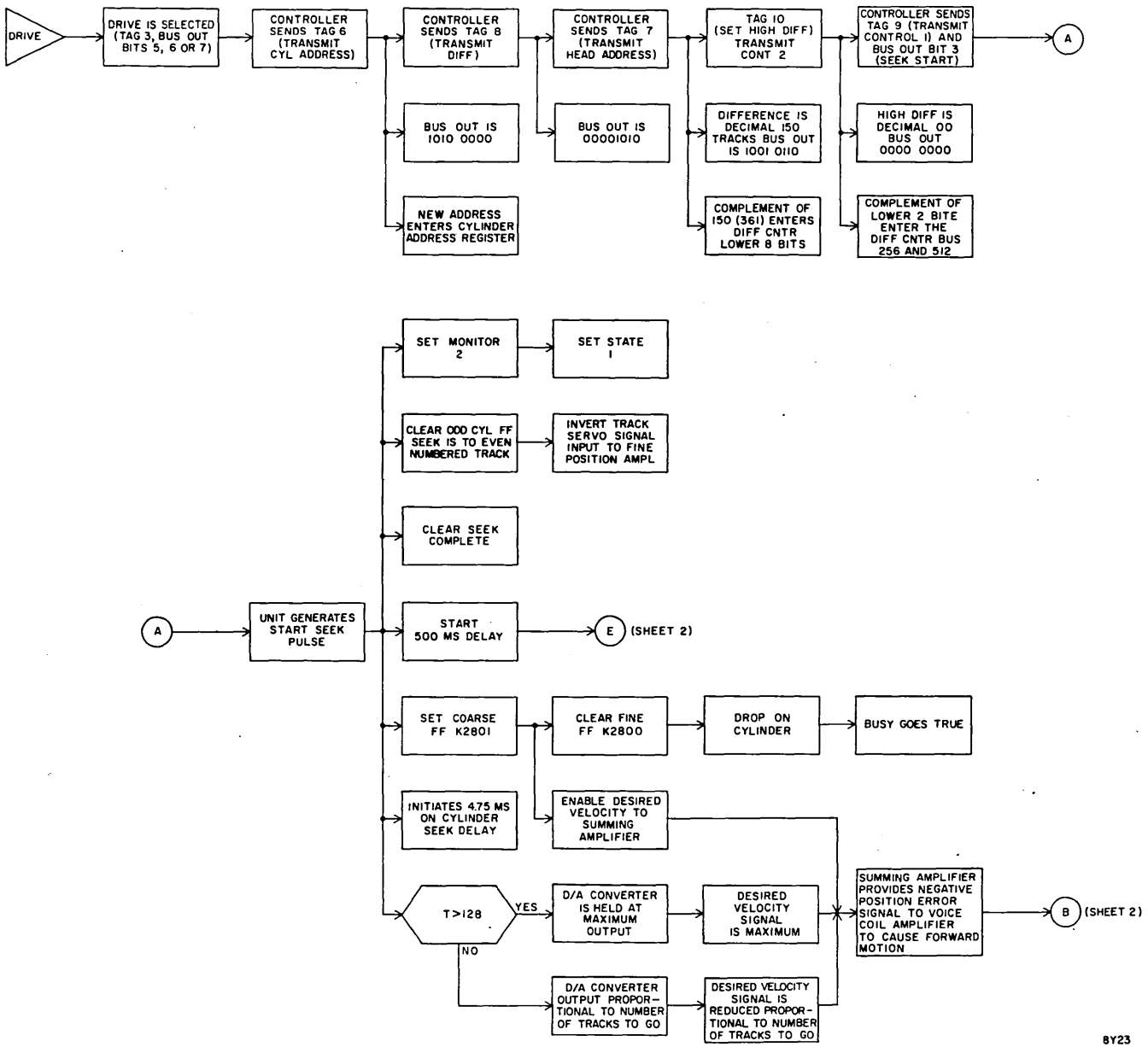


Figure 3-25. Direct Seek Flow Chart (Sheet 1 of 2)

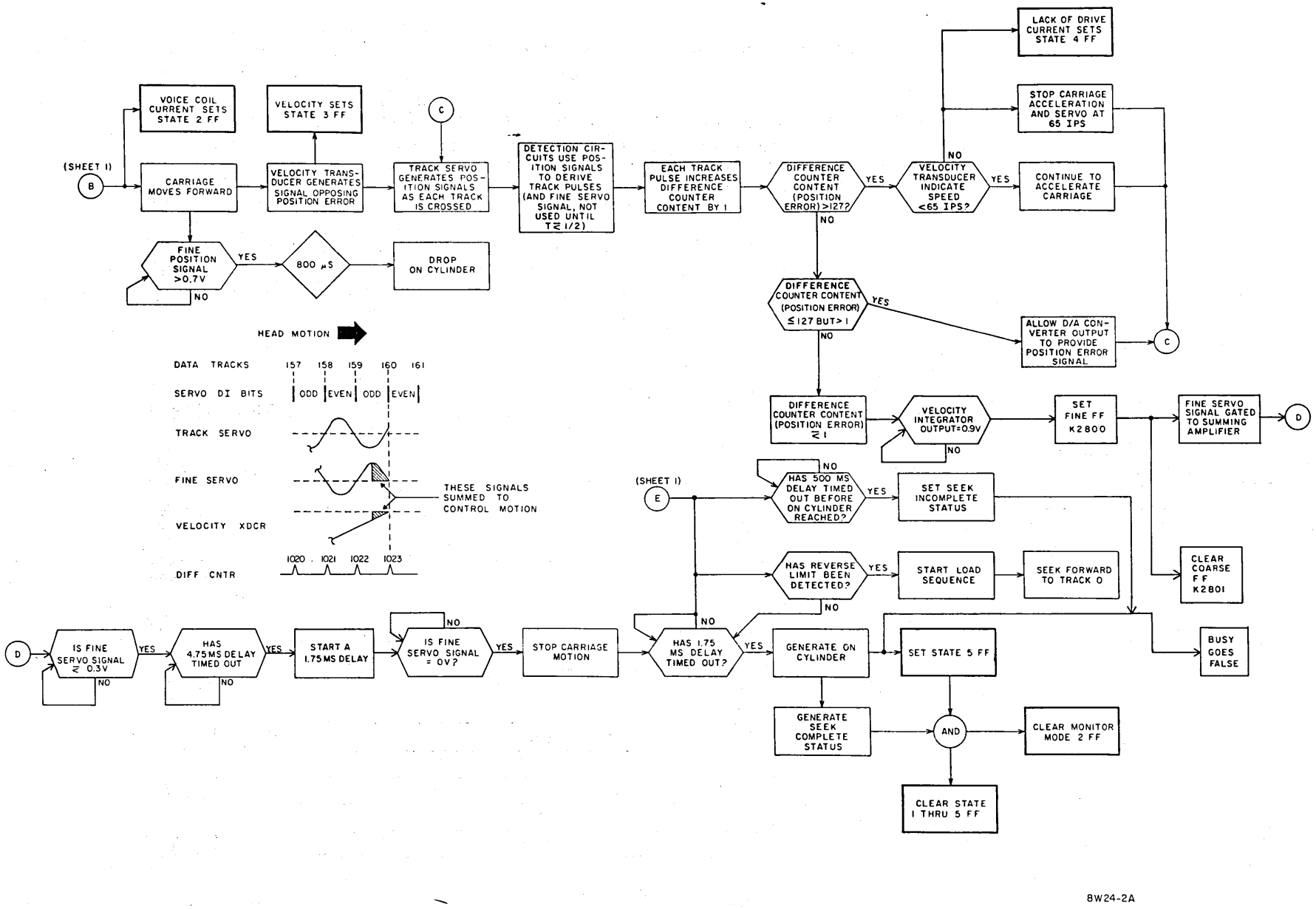
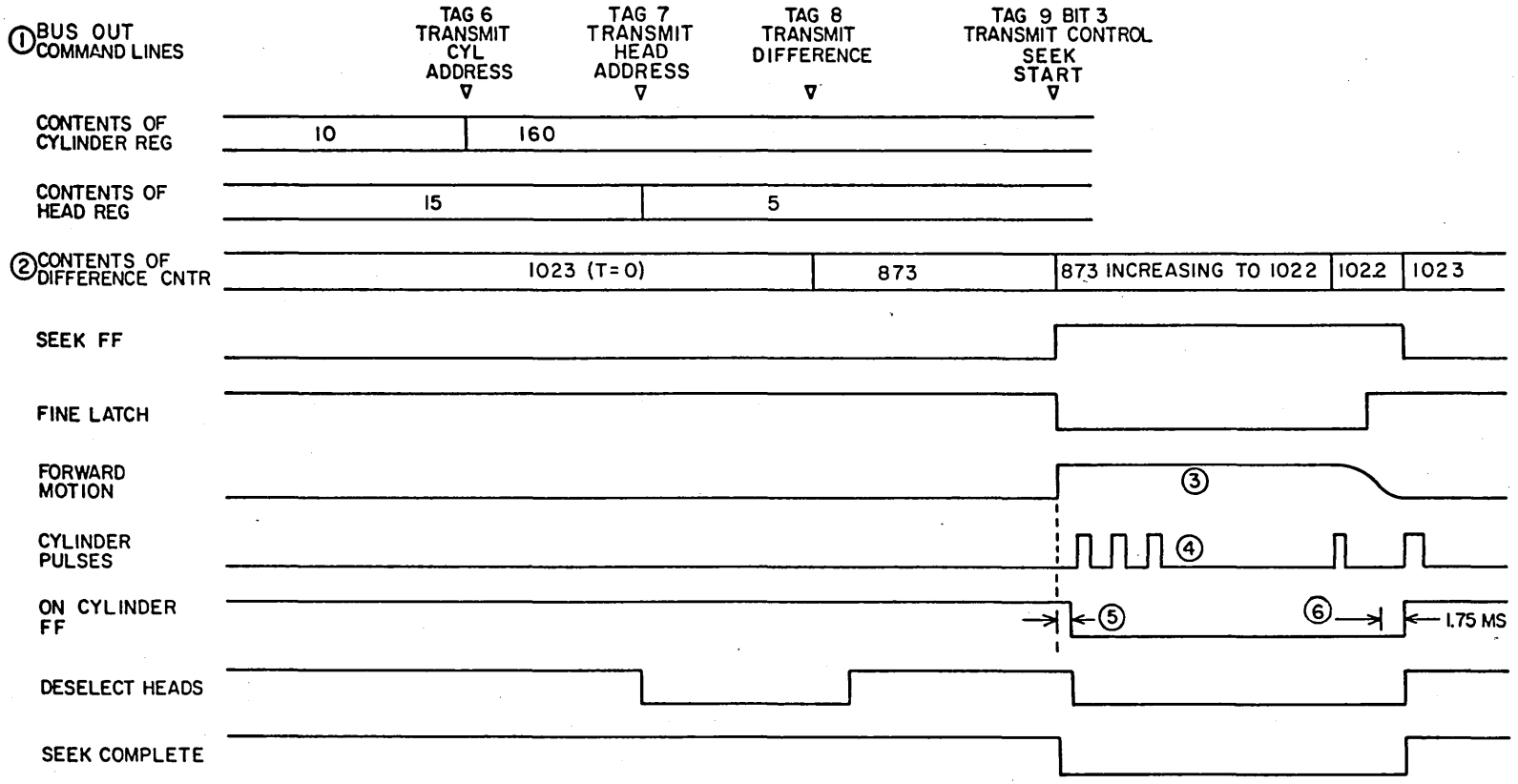


Figure 3-25. Direct Seek Flow Chart (Sheet 2 of 2)



① Device reply not shown. Command loaded at sample time.

② 10 bits of Difference Counter are loaded with the complement of the seek length. The resultant is 873_{10} or complement of 150_{10}, the actual number of tracks to be crossed.

③ Positioner moves forward under control of Position Converter. This signal is maximum until the number of tracks to go is less than 128. At this point it is stepped down under control of the D/A Converter. When approximately 1/2 track remains the Fine FF sets and the positioner is guided on cylinder by the Fine Servo signal.

④ 10 μ sec cylinder pulse generated with each track crossing. First pulse cannot start sooner than .7 msec from seek start.

⑤ On Cylinder drops when Fine FF is cleared.

⑥ On Cylinder Delay starts when fine position becomes less than 0.3v (Assuming that 4.75msec delay has timed out).

8S56A

Figure 3-26. Direct Seek Timing Diagram

6. The following drive events occur with the Seek FF set:

   a. The output of the position converter is gated to the desired velocity function generator to generate the Position Error signal, this initiates voice coil amplifier current.

   b. A 1.2 μsec Start Seek pulse is genrated.

7. Start Seek initiates the following events:

   a. A 500 ms delay is triggered. If On Cylinder is not obtained before the delay times out, Seek Incomplete (BI Tags 9 and 4, Bit 2) is generated.

   b. Bit 2^0 of Cylinder Address register is gated to Odd Cyl FF. If this bit is up, seek is to an odd numbered cylinder. The FF will then be set. The track servo signal is, therefore, inverted before becoming the fine servo signal (position error signal when T<1) during even seeks.

   c. Fine FF is cleared. The position error signal is obtained via the coarse gate.

8. The positioner starts its seek. Refer to Positioner Motion.

9. As the positioner begins to move,the track servo signal increases. This signal functions as the fine position signal in the servo circuit. When it exceeds about 0.7v, On Cylinder Enable drops. The following events occur:

   a. If On Cylinder Enable is down for more than 800 μsec, the On Cylinder FF clears, and the heads are deselected.

   b. The Schmitt triggers driving On Cylinder Enable has hysteresis. Fine position must exceed 0.7v to initiate Not On Cylinder while it must be less than 0.3v to enable the On Cylinder delay.

10. When the seek is completed, Seek Complete Status is generated.

Positioner Motion

The Forward Latch (I1903 and I1904) ANDed with the Seek Latch (I1908, I1909) gates the inverted output of the D/A converter (position error signal) into the desired velocity function generator. (A Reverse FF enable would have gated an uninverted position error signal.) Since the seek length is greater than 127 tracks, the D/A converter output is held at a fixed level by the T>128 signal from the Difference counter. Receipt of the Seek Start signal also caused a Start Seek signal to occur. Start Seek clears the Fine FF, so the output of the desired velocity function generator is gated through the coarse gate to the summing amplifier. Since the carriage is stationary, no velocity signal exists to balance the position error, and forward motion of the positioner begins.

With the position error signal clamped at maximum, the power amplifier output (and voice coil positioner current) will be maximum and the positioner will continue to accelerate. As the positioner moves forward, outputs from the track servo head are processed to derive a cylinder pulse as each cylinder is crossed. Each pulse increases the content of the difference counter by one. As acceleration continues, the velocity signal opposes the position error signal by an increasing amount. The input to the summing amplifier drops off, finally becoming zero when these opposing signals are equal. With a nulled input to the summing amplifier, voice coil current is zero. During this phase, the positioner coasts along the 60 ips plateau with the power amplifier providing only enough output voltage to compensate for the back emf of the moving voice coil positioner.

When the tracks remaining in the seek become less than 128 tracks-to-go, the D/A clamp is disabled for the remainder of the seek (except the last track). As each track is crossed, the D/A converter output steps down by a precise and linear amount. So that the position error provided at the desired velocity function generator input is not also stepped, the integrator clamp gates the velocity integrator on between each cylinder pulse. The resulting integrator sawtooth output is added to the D/A converter output. This removes the step and provides a nearly smooth curve. As the position error decreases, the summing amplifier control signal decelerates the positioner to keep the velocity signal/position error signal difference to zero.

When the counter indicates one track to go to the desired destination (counter=1022) the integrated velocity signal is reset by the regular cylinder pulse. The integrated velocity, which indicates distance, brings up fine enable when about one-half track of travel remains. This sets the Fine FF which, in turn, clears the Coarse FF.

Desired velocity no longer has an effect; the position error is supplied by the fine servo signal. This signal is the track servo signal from the track servo circuit. The amplitude of the signal is proportional to the distance between the present head position and the desired cylinder.

Since the desired destination is track 160, bit 2^0 of the Cylinder Address register is "0". This caused the Odd Cyl FF to be cleared at the start of the seek. As a result, the track servo signal is inverted to form the fine servo signal. In all seeks, the fine servo signal is phased to be opposite to the velocity signal. Since, for forward seeks, the velocity signal is positive-going from a negative value toward zero, fine servo must be negative-going toward zero so that these two signals can oppose each other.

The dibit pattern causes a track servo signal to have a positive slope while approaching an even-numbered cylinder. Therefore, the track servo signal must be inverted to serve as a usable fine servo (position error) signal. If the seek had been to an odd cylinder, Odd Cyl would have been set and the track servo signal would not have been inverted. As the positioner approaches track 160, the fine servo signal approaches 0v. The summing amplifier responds to this decrease in amplitude by decelerating the positioner so that the sum of the velocity and position error equal zero and all motion stops with the servo circuit at null.

With the Fine FF set, the On Cylinder detection circuit is enabled. It receives the analog signal from the fine servo amplifier. When fine servo is less than about 0.3v, the read/write heads are about 0.0003-inch from nominal data track centerline and On Cylinder Enable comes up. If the 4.75 ms delay initiated at the start of the seek has timed out, the 1.75 ms On Cylinder delay is triggered. When it times out, the On Cylinder FF sets and the heads are selected again to permit Read/Write operations.

Since the positioner is not locked by a mechanical mechanism, the servo circuit continues to be enabled following the seek. If the positioner should drift slightly, the track servo signal increases. This signal (fine servo), becomes a position error input to the summing amplifier. This drives the positioner back into place.

Reverse seeks function in an identical manner, except that all phases and polarities are reversed. Total seek times for forward and reverse seeks are identical for seeks of equivalent lengths.

During a Direct Seek operation as during the First Seek operation already considered, a Monitor Mode FF is set. In this case it is the Monitor Mode 2 FF; set by the Start Seek pulse. As the operation continues,State FFs associated with certain events must be set in order. If a State FF is not set or is set out of order, the Device Check FF is set.

RETURN TO ZERO SEEK (RTZS)

The RTZS function is a Seek where the heads are repositioned at Cylinder 000. This function is commanded when the controller issues a Transmit Control I Tag along with bit 4 (Rezero Start). See Figures 3-27 and 3-28 for RTZS timing.

The RTZS pulse sets the RTZ latch and clears the EOT Seek Error and Seek Incomplete FF's. This enables the RTZ gate; this bias voltage forces an average 7 ips reverse motion of the carriage.

When the carriage passes cylinder 000, no more even dibits are detected. This is the Reverse EOT area. The lack of even dibits inhibits cylinder pulses allowing the velocity integrator in the track servo circuit to reach a negative output in excess of 1.28v. This sets the Reverse EOT FF. The integrator is reset, but reverse motion continues unimpeded.

After an additional reverse motion of about two to four tracks, the velocity integrator output again exceeds 1.28v. The RTZ latch is cleared while the Load latch sets. The logic now functions in a manner equivalent to the First Seek sequence.

With the Load latch set, the Load gate supplies a voltage to command a 7 ips forward motion. The velocity integrator, this time indicating forward distance, clears the Load latch to permit continued motion under control of the fine servo signal. The carriage then servoes into cylinder 000.

On Cylinder is available 1.75 ms after the RTZS is completed. The sequence must be completed within 500 ms after RTZS initiation, or else Seek Error is set.

The RTZS function is also used during normal power off sequencing. When the operator presses the START switch, the control interlock opens. This raises the Unload Heads signal in the drive logic. The RTZ latch sets to initiate a 7 ips reverse seek. This

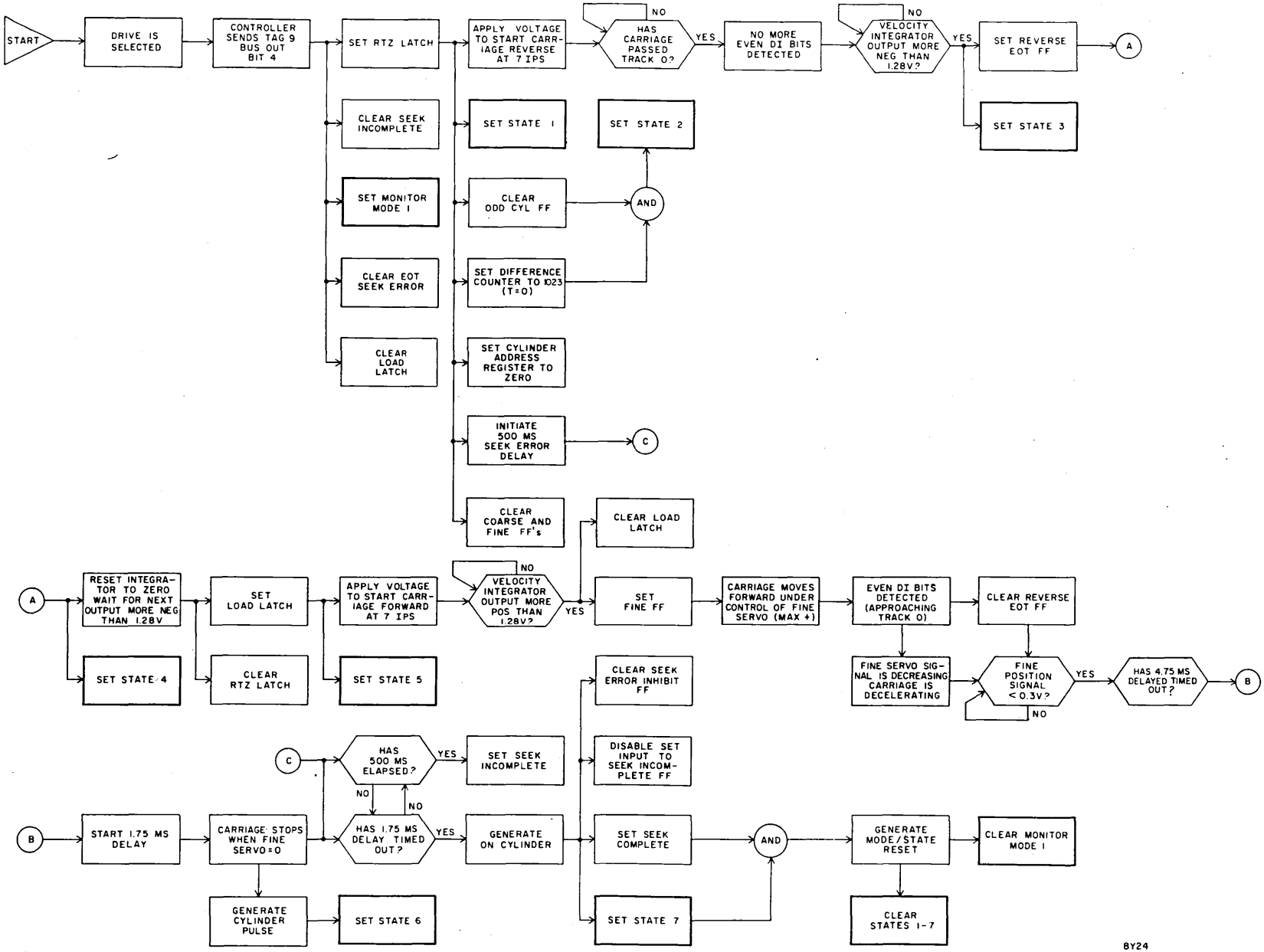
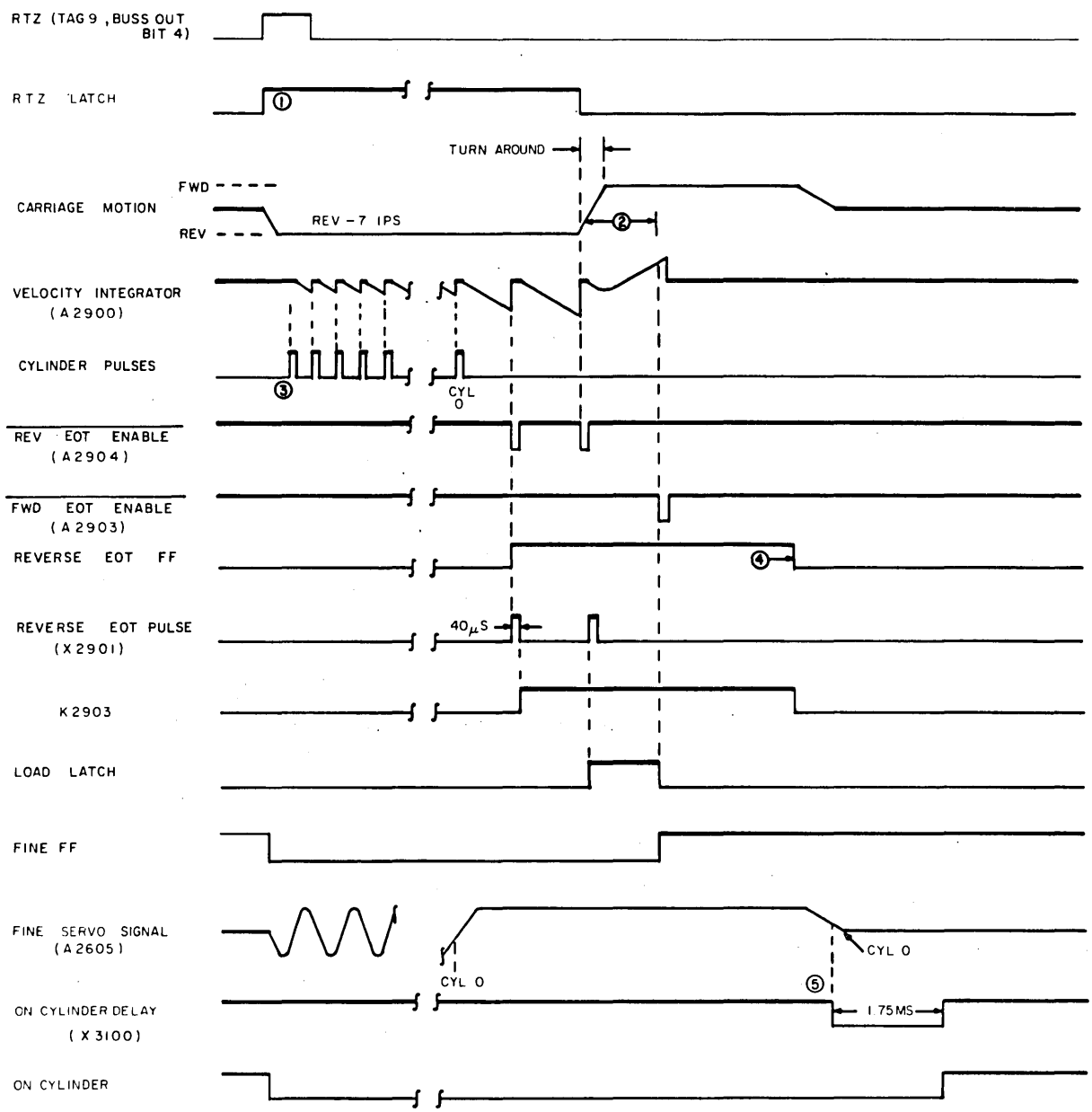


Figure 3-27. RTZS Flow Chart



NOTES:

① RTZ LATCH CAUSES RTZ GATE (A2902) TO APPLY NEG VOLTAGE (SEEK REV) TO VOICE COIL SUMMING AMPL. COARSE AND FINE FF's INHIBITED. CYLINDER REGISTER SET TO ZERO AND DIFFERENCE COUNTER SET TO MAXIMUM (1023).

② FWD MOTION TO 7 IPS PROVIDED BY LOAD GATE (A2903) _ IT PROVIDES + (SEEK FWD) TO SUMMING AMPL. WHEN LOAD LATCH CLEARS, MOTION CONTROL PROVIDED BY FINE SERVO SIGNAL.

③ CYLINDER PULSES RESTART VELOCITY INTEGRATOR. THEY DO NOT AFFECT DIFFERENCE COUNTER.

④ REVERSE EOT FF CLEARED BY FIRST EVEN DI BITS. (APPROACHING TRACK 0).

⑤ ASSUMES 4.75 MS DELAY HAS TIMED OUT.

8Y13

Figure 3-28. RTZS Timing Diagram

time however, the EOT Enable circuit is disabled so that the EOT integrator signal has no effect. In turn, the Load latch is disabled. Reverse motion continues until the heads unload. A Select Lock condition does not inhibit the unloading; however, unloading does not clear the SELECT LOCK indicator.

The RTZS function occurs automatically in the heads unloaded condition if dibits are lost for more than 200 ms. The Select Lock FF is set to prevent another First Seek until the SELECT LOCK indicator has been cleared.

MACHINE CLOCK CIRCUIT

The machine clock circuit uses dibits generated by the track servo circuit to generate the basic 806 kHz clock signal. This signal is applied to the following circuits:

1. Index detection
2. Write clock generator
3. Sector counter

Clock Generation

The circuits (Figure 3-29) most important portion is a phase locked loop (PLL). The loop compares the frequency of input data (dibits) with feedback data. A comparator circuit generates a square wave input to a GJK circuit in the voltage controlled oscillator. (Refer to Section 6 for an explanation of the GJK circuit.) The GJK generates a voltage proportional to the difference in frequency between input data and feedback data. The output of the GJK is applied to the voltage controlled oscillator to control its frequency. The PLL is satisfied when the input and feedback frequencies are identical. Note that data and feedback are 90 degrees out of phase.

There are three inputs to the comparator. One is the normal input from dibits delayed approximately 1/4 cell and shaped to 30 nsec (approximate) pulses. The second input is a dub-in input. This is a 30 nsec pulse coming up at the same time as the normal input but from the clock output. The third input

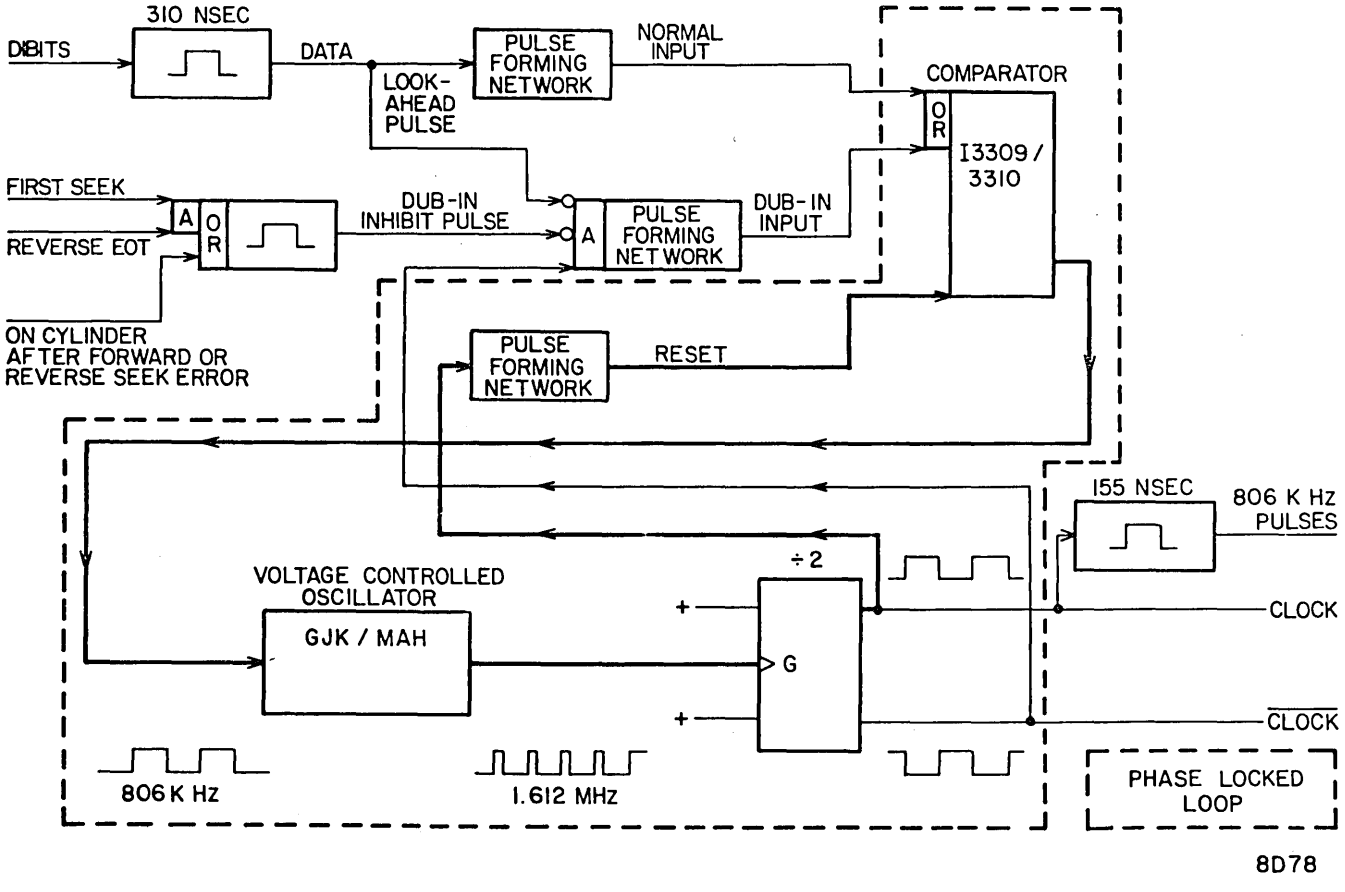


Figure 3-29. Machine Clock Circuit

is the reset pulse. It is the normal and the reset input which provide the basis for normal comparator operation.

During normal operation, a look-ahead pulse blocks the dub-in input to the comparator. This insures that the comparator and therefore the clock, tracks with the real input data from dibits. However, if dibits are missing, as they are during the Index mark (for two cells) or during a seek (every other cell), there must be a pseudo-dibit or dub-in pulse to keep the clock in phase. Therefore, the circuit is self-ringing when data is not present at the input.

A problem with the self-ringing feature of the circuit is that, if the first input to the comparator is not data but a dub-in pulse, the circuit may not be in synchronization with real data when it is received. It would then take some time before synchronization could be attained. The 5 ms dub-in inhibit pulse fires to block dub-in pulses in three situations: 1) when the latch is cleared by reverse EOT at the end of a first seek, or 2) and 3) when On Cylinder is received after a forward or reverse seek error.

After the heads are loaded, even/odd dibits are available. Their nominal frequency is 806 kHz. The actual frequency is a function of spindle motor speed. The PLL quickly synchronizes itself to the actual dibit rate. This permits the clock to react to variations in spindle speed between drives. Signals derived from this circuit, such as sectors, are a function of actual spindle speed rather than functions of an absolute time base.

FF K3301 is connected as a divide-by-two circuit. This circuit arrangement permits the PLL feedback to be a function of negative-going edges of the PLL output. Therefore, PLL unsymetrical outputs are ignored and the basic frequency is the controlling factor. The PLL output frequency is nominally 1.612 MHz.

Index Detection Circuit

The Index Detection circuit (Figure 3-30) generates a 2-µsec pulse at the start of each new logical track. This signal is returned to the controller as Index (BI Bit 5) and also resets the sector counter to zero.

Prior to reaching the Index area, both even and odd dibits are available. Dibits Present FF (K3401) is held in the preset state: this causes the counter to be continually loaded with zero with each clock pulse from X3400. The counter can continue to increment only if the precise pattern continues to be sensed. Any other combination of missing dibits (such as when tracks are crossed during seeks) will cause the counter to be reset to zero.

When the counter reaches a decoded value of 550, two of the three input gates to Index Detect FF K3402 are available. The next even dibit triggers X3400 to set the FF. In turn, X3401 provides a 2-µsec Index pulse.

Note that Index is inhibited while the heads are over either a forward or reverse EOT area.

Index Error Detection

The Index signal must appear between count 50 of the last sector (127) and count 4 of the first sector (000). If the Index pulse is not detected at this time, the Index Error FF will set. Refer to Figure 3-31.

During normal operation, the Not Index Window FF receives gating pulses at each sector count of 4 and 50. The FF does not toggle however, until sector 127. When sector 127 is reached, count 50 clears the FF. The next count 4 (sector 000) sets the FF. During the time the FF is cleared, the Index pulse will be received. The Index pulse, combined with the clear output of the Not Index Window FF, sets the Index Detected FF. The next count 23 resets the Index Detected FF.

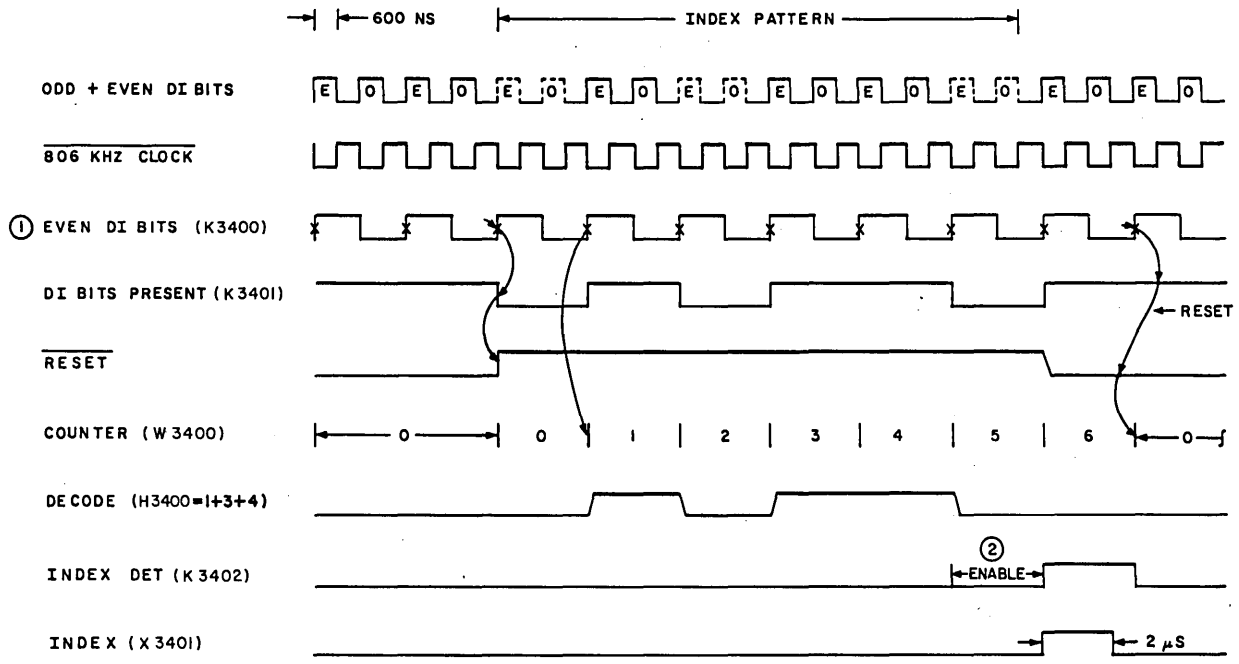
If Index is received when the Not Index Window FF is set (an error condition) it enables a gate to the Index Error FF and force sets it. On the other hand, if no Index pulse is received when the Not Index Window is cleared, the Index Error FF is set. An Index Error raises Bus In, Bit 0 if Tags 4 or 9 are decoded.

Sector Circuit

The sector circuit (Figure 3-32) permits the controller to determine the current angular position (sector) of the read/write heads with respect to Index. The circuit may also be used to set up an Interrupt signal when a sector requested by the controller is reached. Each track may be considered as subdivided into 128 segments. They are numbered from 000 to 127. Sector 000 is the first sector following Index.

The circuit consists of three major elements:

1. A Clock Counter to count even dibits.
2. A Sector Counter that maintains a continuous count of the current sector.
3. A Sector register used to supply Record Ready Interrupt or to provide the controller with the current sector count.



NOTES:

① X INDICATES LEADING EDGE OF SINGLE SHOT X3400

② NEXT LEADING EDGE REQUIRED TO SET FF BECAUSE OF PROPAGATION TIME THRU H3400/K3402

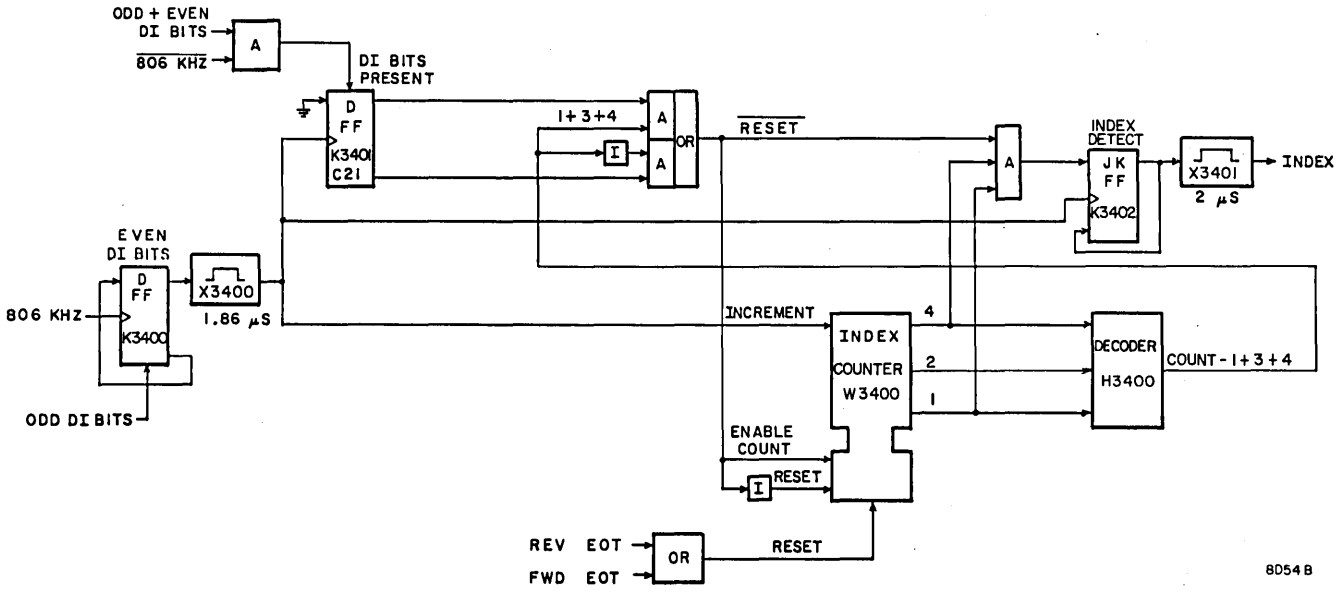


Figure 3-30. Index Detection Circuit

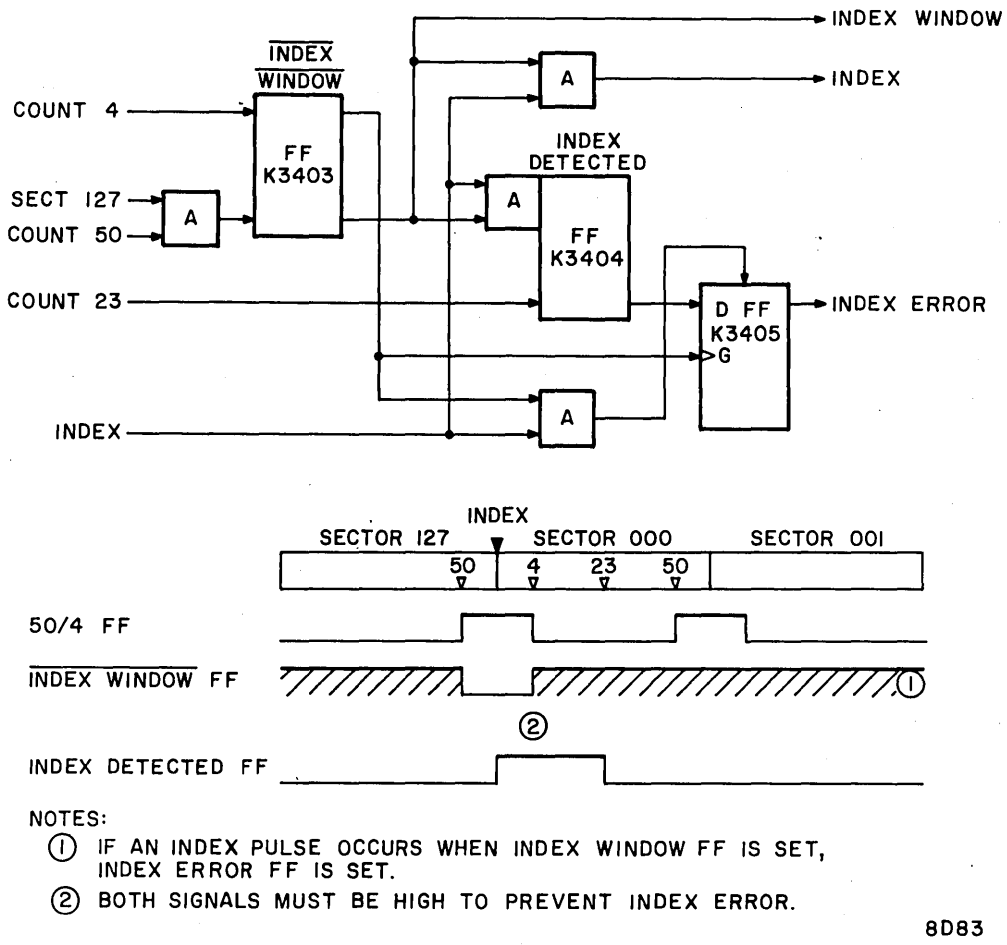


Figure 3-31. Index Error Detection Circuit and Timing

The 806 kHz clock signal is used to generate the sector count. An Index pulse sets the Even Sector FF and partially enables the Clock counter input. The first even clock signal then loads the clock counter. Each positive-going (even) clock pulse increments the clock counter. When the clock counter counts 53 even pulses, the sector counter is incremented by one and the clock counter is reset. Each time the clock counter is reset, the Even Sector FF changes state. Note that the count loaded when an odd sector is to be counted is one greater than for an even sector. This is because an odd sector has one less clock bit per sector than does an even sector.

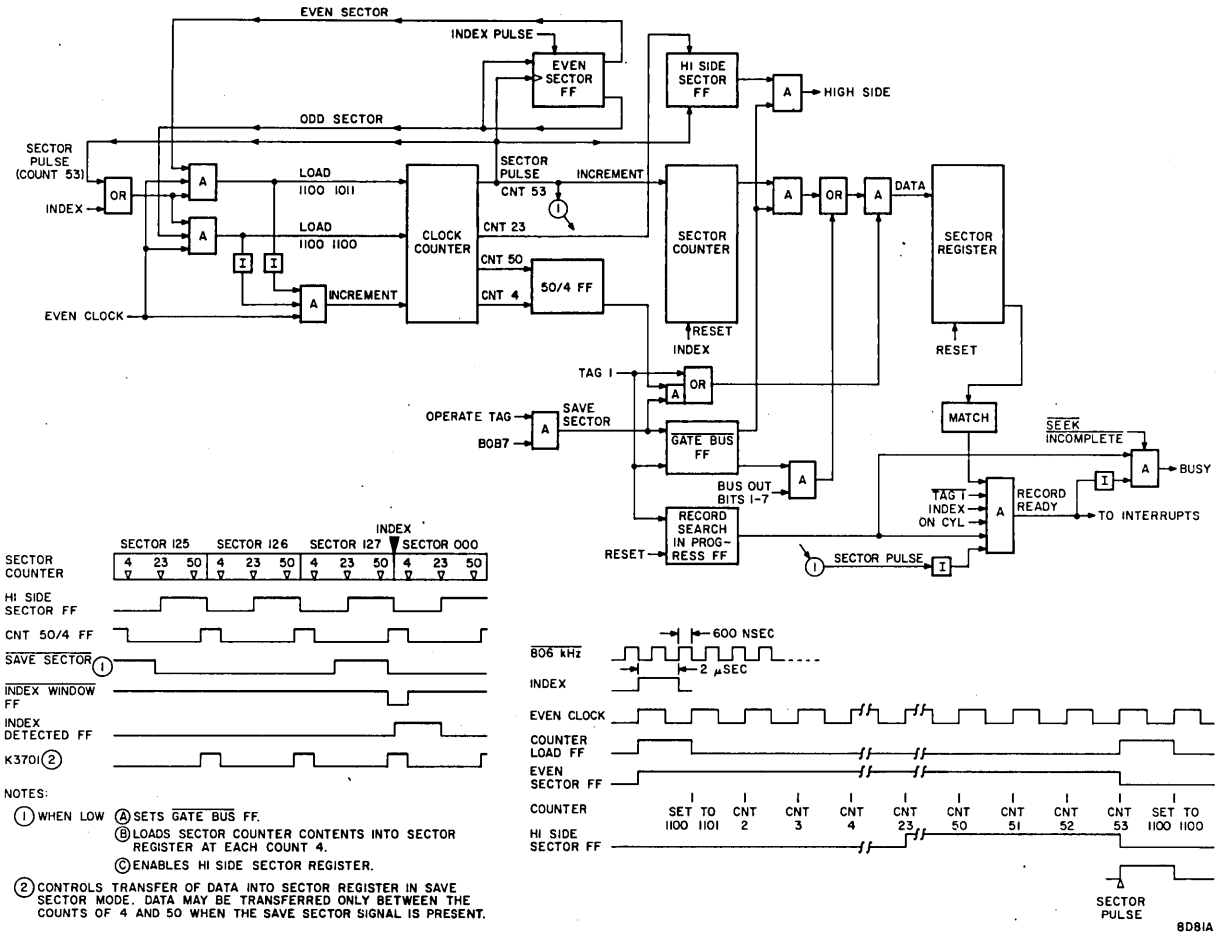
As the clock counter proceeds, the following counts are important:

Count 4 - Clears the 50/4 FF and acts as a partial enable for data input to the Sector register.

Count 23- Sets the Hi Side Sector FF.

Count 50- Sets the 50/4 FF.

Count 53- Clears the Hi Side Sector FF, toggles the Even Sector FF and increments the Sector Counter.



NOTES:

(1) WHEN LOW (A) SETS GATE BUS FF.
(B) LOADS SECTOR COUNTER CONTENTS INTO SECTOR REGISTER AT EACH COUNT 4.
(C) ENABLES HI SIDE SECTOR REGISTER.

(2) CONTROLS TRANSFER OF DATA INTO SECTOR REGISTER IN SAVE SECTOR MODE. DATA MAY BE TRANSFERRED ONLY BETWEEN THE COUNTS OF 4 AND 50 WHEN THE SAVE SECTOR SIGNAL IS PRESENT.

Figure 3-32. Sector Circuit

The Sector counter continues to count until reset by an Index signal. When enabled, the contents of the Sector counter is transferred to the Sector register. To load the Sector register from the Sector counter, the unit must receive Tag 11 BOB7 (Save Sector). The next count 4 of the clock counter will load Sector counter contents into the Sector register. From then on, the register is continually updated by the Sector counter until the next Tag 1.

Data may also be placed in the Sector register directly from the counter. Tag 1 BOB1-7 loads a sector count directly into the Sector register. After the controller loads the Sector register, a compare circuit compares the output of the Sector counter and the contents of the Sector register. When a match occurs, a Record Ready signal is generated if the following additional conditions are met:

1. Record Search in Progress FF set.
2. Tag 1 (Transmit Sector) low.
3. On Cylinder.
4. Neither an Index nor a Sector Pulse may be present.

A Record Ready signal drops the Busy signal and generates an Interrupt when the device is polled.

SENSE OPERATIONS

Sense operations permit the controller to determine drive status.

Device Check

Refer to simplified logic (Figure 3-33). The Device Check logic signals the controller by raising the Device Check line if any of the following error conditions occur:

1. The controller commands a Seek operation when a Seek operation is illegal. Refer to Seek operations.
2. The controller commands Head Advance at end of cylinder or a Write operation during an Offset or a Not Tag 11. Valid signal is received from the Fault Detection circuit.
3. Any of the Monitor Check signals (refer to Maintenance Monitor).
4. A Test Logic signal (Tag 12,BOB6) forces a Device Check signal.
5. Select Lock or Interface Check signals besides raising their own identifying bits, also set the Device Check FF.

One and two above also raises the Command Reject line to the controller.

Maintenance Monitor

Three of the seek operations we have considered, First Seek, Direct Seek, and Return to Zero Seek, are monitored during their normal operation by the Maintenance Monitor circuitry. Besides the three seek Monitor Modes, both the Read and Write operations are monitored.

The operation of all Monitor Modes is basically the same. At the beginning of the monitored operation, the Mode FF or FFs are set by the internal logic signal which begins the operation. Mode FFs can also be set by commands from the controller as part of a diagnostic procedure. Once set, the Monitor Mode FFs act as enables to the Monitor State latches. Thereafter, each event during the operation sets the appropriate State FF. Refer to the Seek flow charts for examples. Assuming all events progress normally, at the end of the operation all State FFs associated with the operation mode are set. The final event of the operation (Seek Complete for Seek operations, not read for read operations and not write for write operations) sets the Mode/State Reset FF and clears all Mode and State FFs.

Monitor mode error detection is accomplished in two ways. State FFs set out of sequence or skipped in sequence are detected as state errors and raise the Monitor Check signal immediately. However, if the State FFs are set in order but for some reason one or more of the State FFs is not set, the Monitor Check signal is not raised immediately. The signal will be raised in the seek operations when On Cylinder is detected. In the Read or Write operations, Monitor Check is raised at the end of the operation, when the Operate (Tag 11) line drops. Clearing the Monitor Check FF raises the Monitor Check signal, raises the Device Check signal, and holds the Mode and State FF's in their last state.

A Spike Detect signal from the Desired Velocity circuit during a Direct Seek operation is immediately detected as an error. During a Write operation, State 4 through 8 FFs are set by error conditions rather than normal operation. The errors detected are:

1. Write and Offset Active both selected (State 4)
2. An AC Write Fault (State 5)
3. Simultaneous Read and Write (State 6)
4. Write selected AND (Not On Cylinder OR Not Head Selected OR EOC) (State 7)
5. A Multiple Head Select or Current Fault (State 8)

Five above is also detected as an error during a Read Monitor operation.

DIAGNOSTICS

The Diagnostic circuitry allows maintenance personnel to check out key portions of the drive logic. State diagnostics check servo loop operation with only simulated drive commands and no actual carriage or disk motion. Dynamic diagnostics monitor drive during normal on-line operation. The application of drive diagnostic functions is entirely a function of microprogram firmware/software and is described by the microprogram description in the controller manual.

Static Diagnostics

Drive is powered down. The Unload Heads signal is inhibited and a false On Cylinder Status is set. Now either a direct or RTZ seek may be simulated by a series of enabling signals from the controller. These enabling signals call for the servo loop to respond

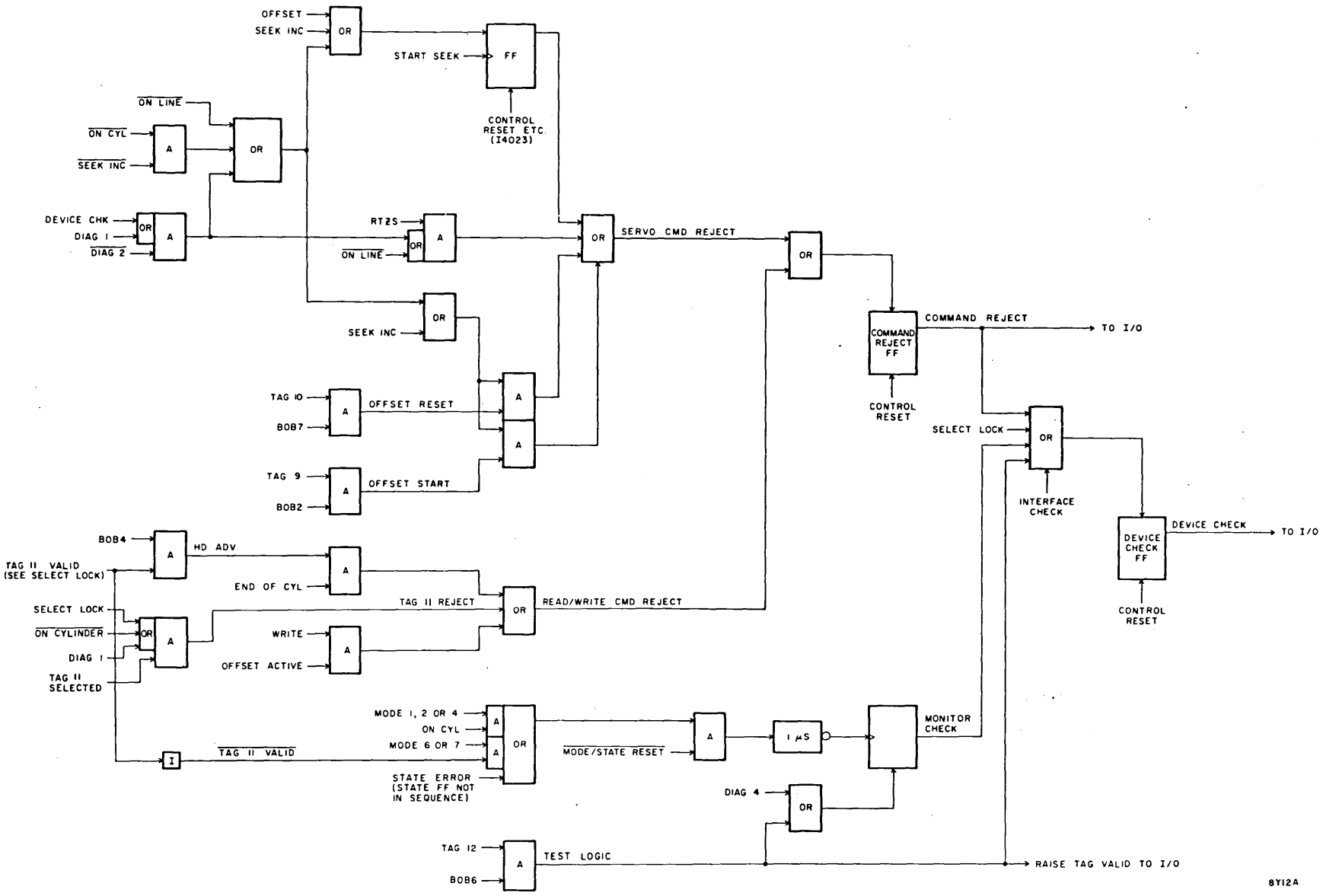


Figure 3-33. Device Check Logic

to portions of the seek routines as if normal motion were taking place. The Monitor Mode logic is operative as a normal operations and successful completion of each portion of the simulated seek is indicated by setting the applicable State FF.

Dynamic Diagnostics

Dynamic diagnostics differ from Static diagnostics in that there is drive motion. By application of pertinent commands (Request Diagnostic Sense, Tag 12) drive status may be monitored. Also, errors can be intentionally introduced (for example, simultaneous Read and Write commands) to ensure correct response of error detection circuits.

Diagnostic Entry

The Diagnostic mode is set by Tag 13 from the controller. One or more of three latches can be set with this command. Each of the latches enables or inhibits certain events to allow illegal commands or events to take place. The latches and their associated events are:

- Diagnostic 1 (Tag 13 BOB3)
  1. Inhibits set input to Cylinder Address register.
  2. Inhibits set input to Difference counter.
  3. Inhibits the set input to the Head Address register.
  4. Inhibits any operation prefaced by Tag 11.
- Diagnostic 2 (Tag 13 BOB2)
  1. Partially inhibits Servo Command Reject.
  2. Enables Static Diagnostics by making the Request Status bits (Tag 4) significant.
  3. Enables a multiple head fault by selecting two heads when a head address greater than 18 is selected.
  4. Enables a loss of dibits causing the heads to react and setting the Select Lock FF when combined with Tag 4, BOB6.
- Diagnostic 4
  1. Forces an index error condition by presetting a count of 8 into the dibit counter. This causes Index Window to be generated approximately 1.4 sectors prior to actual Index.
  2. Enables Read Gate Lock up. Normally the Read Gate is dropped each time the Head Select signal is dropped. Selecting Diagnostic 4 however, holds the Read Gate high. This lockup mode is cleared by applying an AM Search signal or clearing Diagnostic Mode 4.

The following flow charts (Figure 3-34 and 3-35) cover one basic diagnostic procedure. Note their dependence on controller commands. For this reason these flow charts should be used as guides only. Specific information regarding diagnostic procedures will be found in the controller manual.

BASIC READ/WRITE PRINCIPLES

Introduction

Information is recorded on, and read from, the disk pack by means of 19 heads. Each head contains a read/write coil.

Writing Data

Data is written by passing a current through a read/write coil within the selected head. This generates a flux field across the gap in the head (Figure 3-36). The flux field magnetizes the iron oxide particles bound to the disk surface. Each particle is then the equivalent of a miniature bar magnet with a North pole and a South pole. The writing process orients the poles to permanently store the direction of the flux field as the oxide passes beneath the head. The direction of the flux field is a function of Write current polarity while its amplitude depends upon the amount of current: the greater the current, the more oxide particles are affected to the point of saturation.

Information (data) is written by reversing the current through the head. This change in current polarity switches the direction of the flux field across the gap. The flux change defines a data bit.

Reading Data

As the disk passes beneath the read/write head, the stored flux intersects the gap (Figure 3-37). Gap motion through the flux induces a voltage in the head windings. This voltage is analyzed by the read circuit to define the data recorded on the disk.

Each flux reversal (caused by a current polarity change while writing) generates a readback voltage pulse. Each pulse,in turn, represents a data bit.

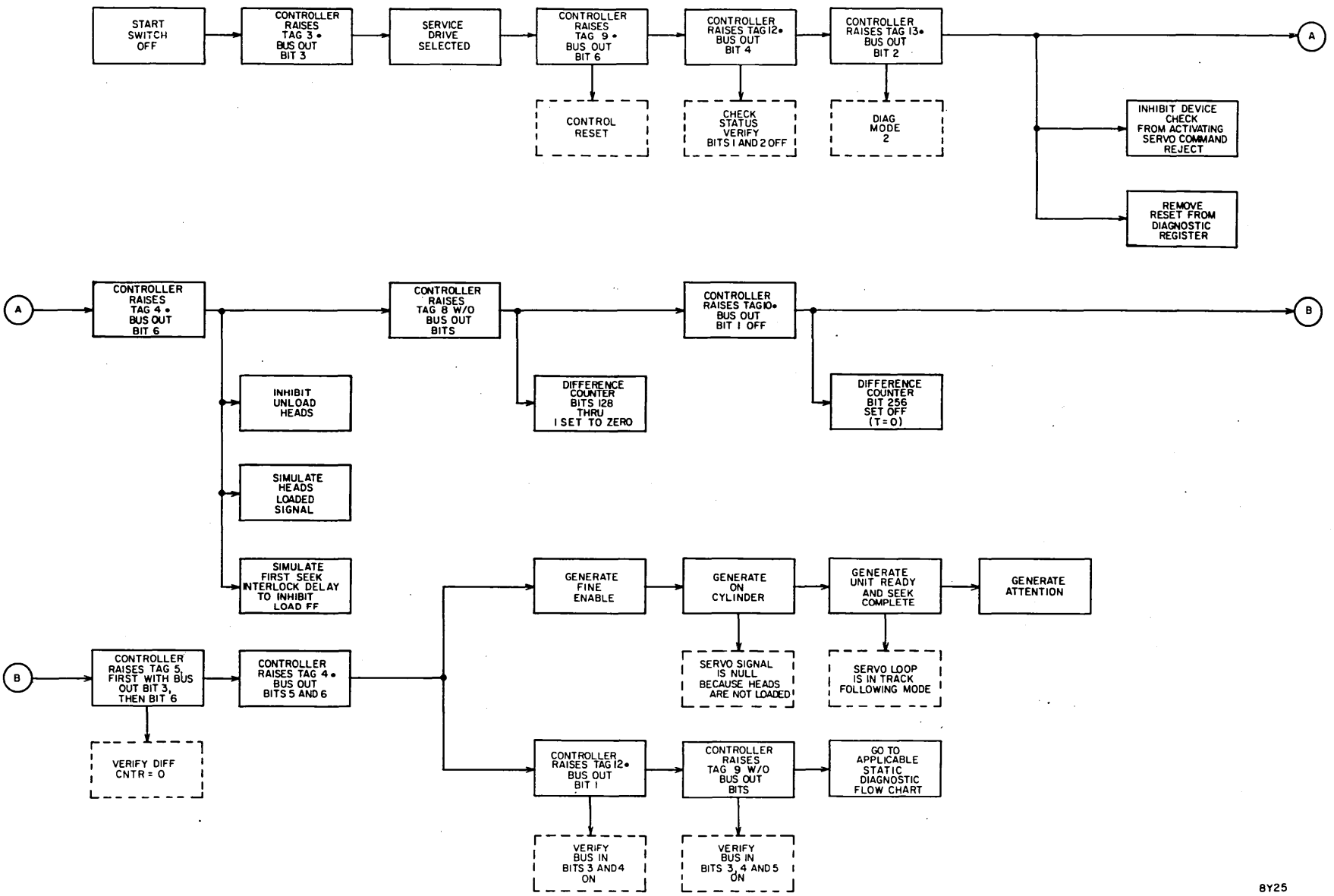


Figure 3-34. Static Diagnostics Entry Flow Chart

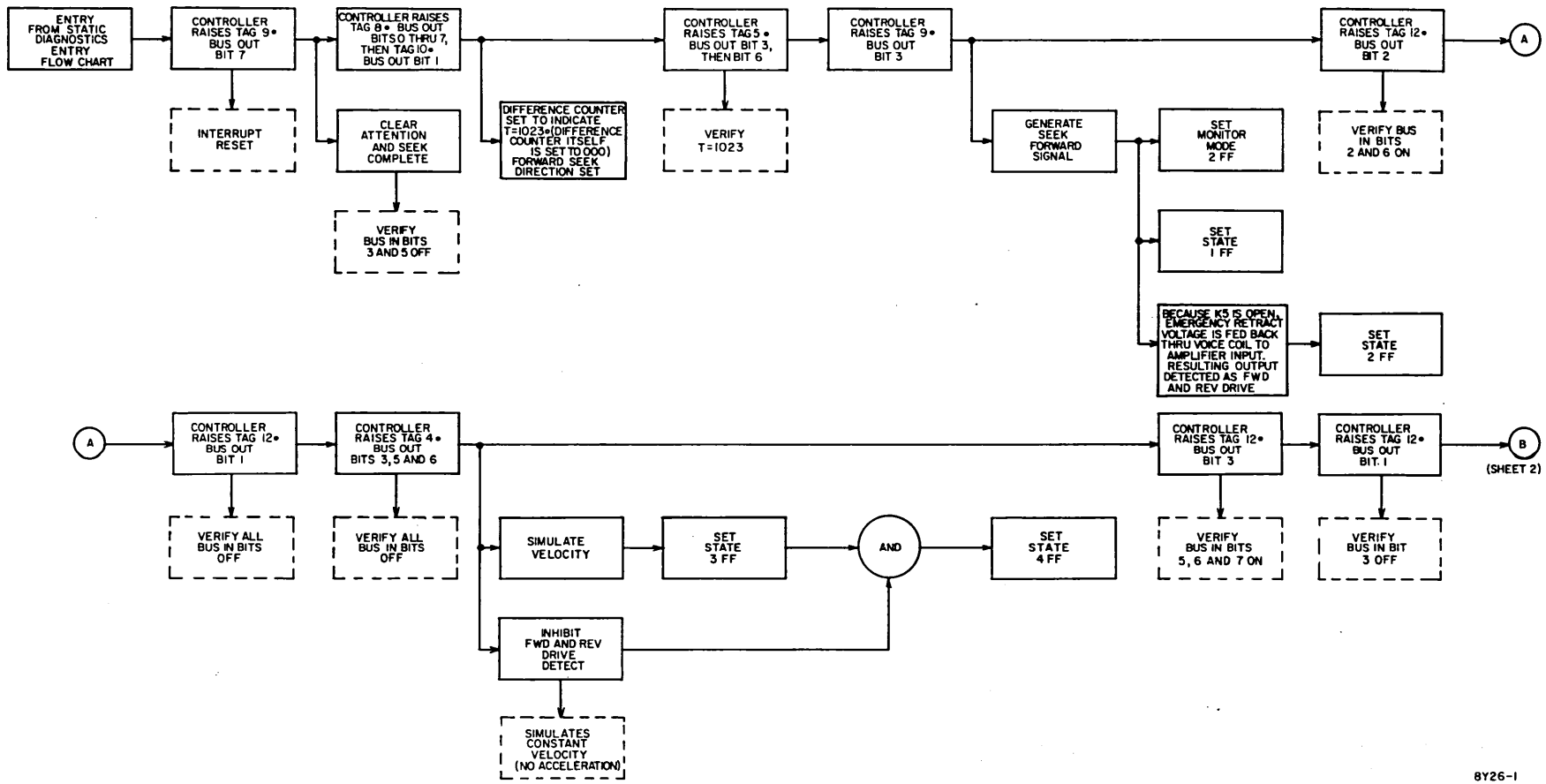


Figure 3-35. Static Diagnostic Flow Chart (Sheet 1 of 2)

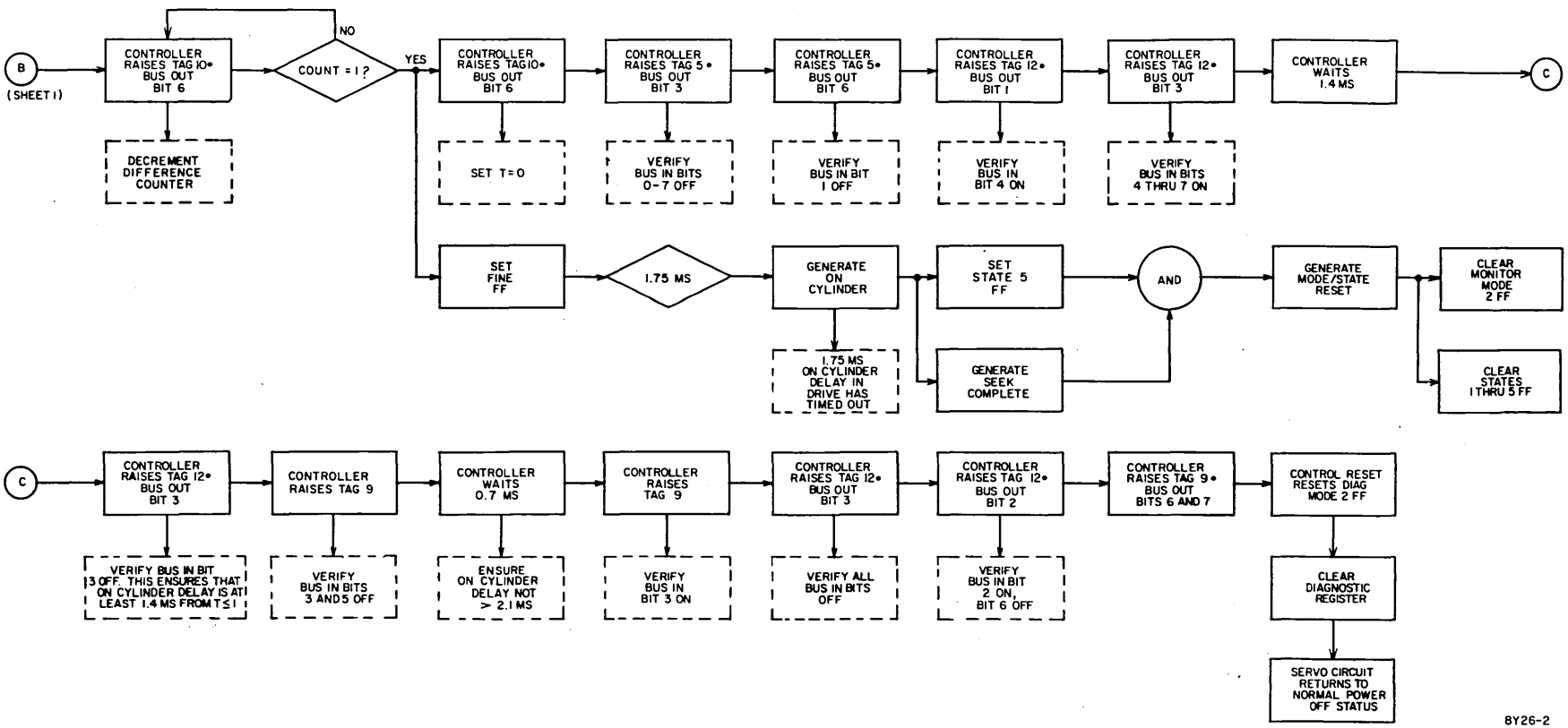


Figure 3-35. Static Diagnostics Flow Chart (Sheet 2 of 2)

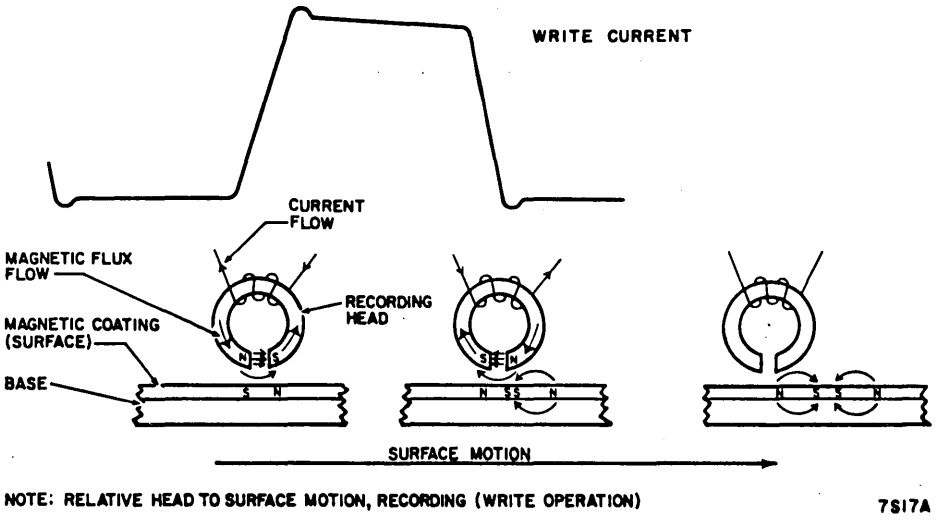


Figure 3-36. Writing Data

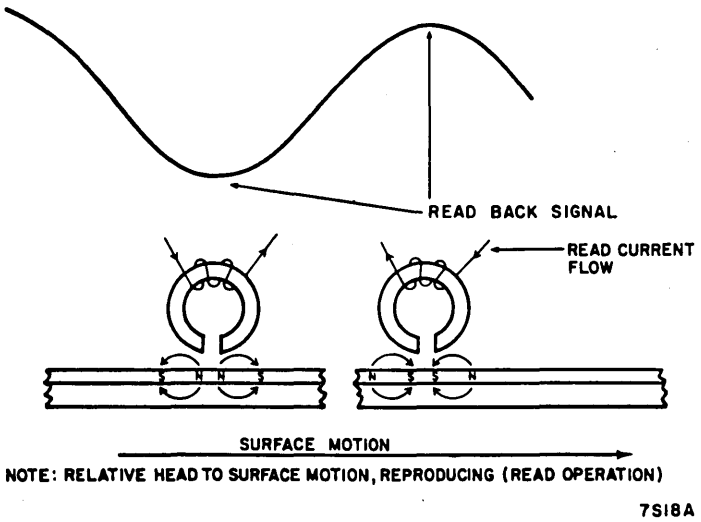


Figure 3-37. Reading Data

Track Format

Each track has Index as its starting point. The track is further subdivided into 128 sectors. Sector 00 is the first sector following Index. Index and On Sector signals are available to the controller. For further information, refer to the Direct (Forward/ Reverse) Seek theory in this section.

One track is operated upon by one read/write head. The heads are numbered from 0 to 18. These heads are positioned vertically with respect to each other. As a result, all 19 of the heads may be used without moving the actuator. Since any of the heads may be addressed at practically instantaneous rates, the recording medium may be thought of as a cylinder rather than as 19 discrete surfaces. This is the cylinder concept. Since the actuator may be positioned horizontally to any one of 823 rings or tracks, there are 823 cylinders. They are numbered from 000 (the cylinder nearest the outside edge of the disk) to 822 (the innermost cylinder). Any track may be addressed by seeking to the desired cylinder and by selecting one head. Only one head may be selected at a time.

Track format, sector control, and data record format are functions of the operating system. These functions are directly controlled by the controller. Refer to the applicable controller manual for further information.

Principles of MFM Recording

In order to define the binary digits stored on the pack, the frequency of the flux reversals must be carefully controlled. Several recording methods are available; each has its advantages and disadvantages. This unit uses the Modified Frequency Modulation technique.

The length of time required to define one bit of information is the cell. Each cell is nominally 155 nsec in width. The data transfer rate is, therefore, nominally 6.45 MHz.

MFM defines a "1" by writing a pulse at the half-cell time (Figure 3-38). A "0" is defined by the absence of a pulse at the half-cell time. A pulse at the beginning of a cell is Clock; however, Clock is not always written. Clock is suppressed if there will be a "1" in this cell or if there was a "1" in the previous cell.

The rules for MFM recording may be summarized as follows:

1. There is a flux transition for each "1" bit at the time of the "1".
2. There is a flux transition between each pair of "0" bits.
3. There is no flux transition between the bits of a "10" or "01" combination.

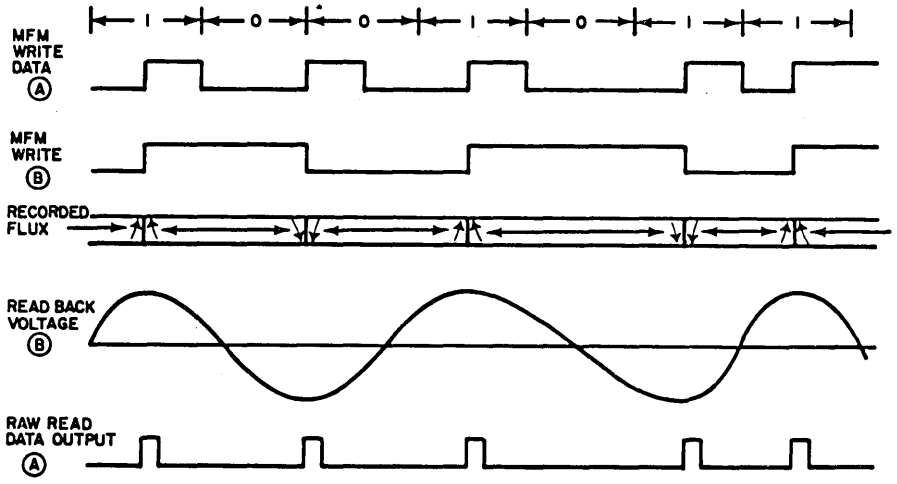


Figure 3-38. MFM Recording

The advantages and disadvantages of MFM recording are as follows:

1. Fewer flux reversals are needed to represent a given binary number because there are less flux reversals at the cell boundaries. This achieves higher recording densities of data without increasing the number of flux reversals per inch.

2. Signal-to-noise ratio, amplitude resolution, read chain operation, and operation of the heads are improved by the lower recording frequency achieved because of fewer flux reversals required for a given binary number.

3. Pulse polarity has no relation to the value of a bit without defining the cell time along with cell polarity. This requires additional read/write logic and high quality recording media to be accomplished.

READ/WRITE OPERATIONS

Introduction

An overall block diagram of the read/write chain is shown in Figure 3-39. More detailed block diagrams and timing diagrams are shown in conjunction with the discussions of the various stages in the read/write chain.

Head Selection

The Head Selection circuit must select the desired head before a Read or Write operation can be performed. The head selection process is initiated by a Transmit Head Address command (Tag 7) from the controller. This code gates the desired head address into the Head Address register (Figure 3-40). For purposes of this discussion, assume that head 02 is the head to be selected.

Bit 1 of the Head Address register (set by Tag 7 BOB7) determines if the head selected will be odd or even. Since in this example bit 1 is off, an even head is selected. Bus Out Bit 6 on, with BOB7 off activates Even Heads Bit 0. Assuming Head Select enable (Tag 11, BOB3) is present, Head 02 is enabled by applying a ground to the read/write head center tap.

Note that if the selected head number is decimal 19 or greater, an End of Cylinder signal is generated. This deselects all heads. The content of the Head Address register can be increased by one by a Head Advance function code (Tag 11 BOB4) from the controller.

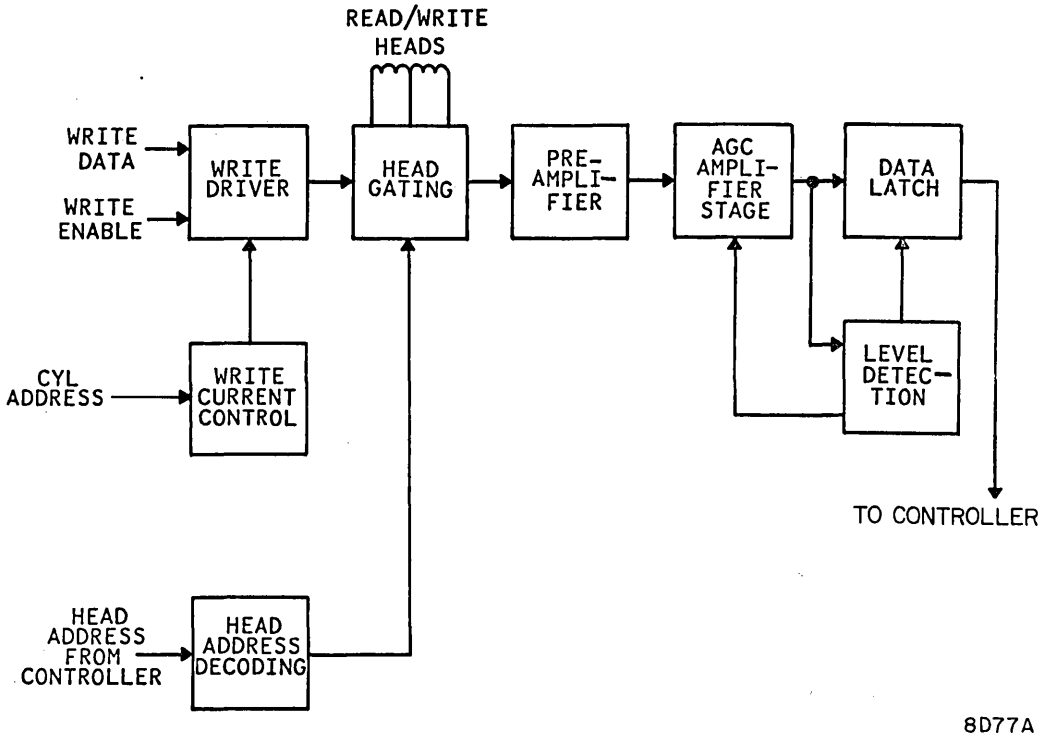
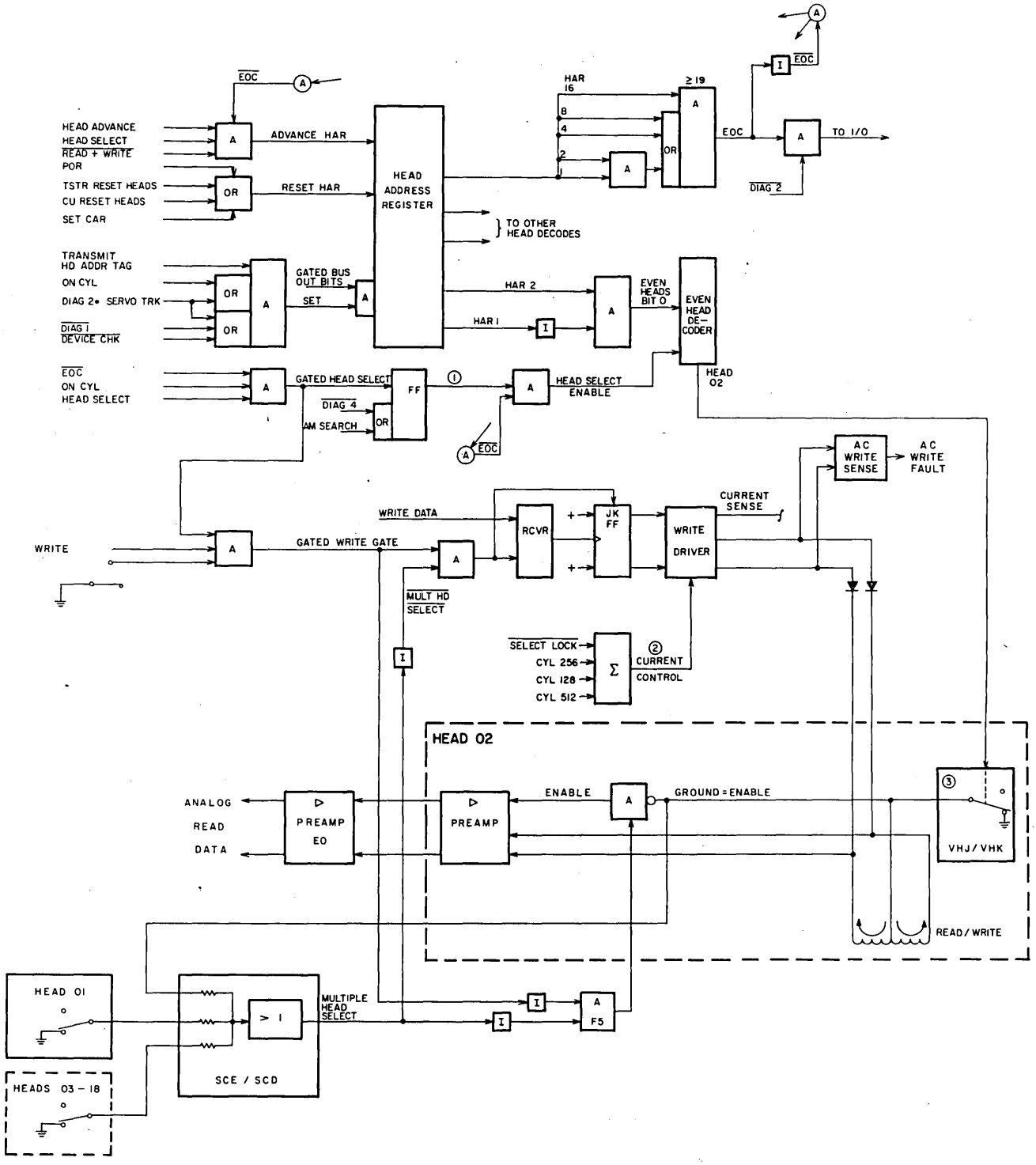


Figure 3-39. Read/Write Chain Block Diagram



NOTES:

(1) THE FF CAN BE SET ONLY BY GATED HEAD SELECT. ONCE SET HOWEVER THE SET STATE MAY BE MAINTAINED BY DIAG 4 STATE AND AM SEARCH. THE FF IS CLEARED WHEN GATED HEAD SELECT IS DROPPED AND AM SEARCH OR DIAG 4 IS PRESENT.

(2) DECREASES WRITE CURRENT AS HEADS ARE CLOSER TO SPINDLE. CURRENT IS GREATEST AT CYLS 0-127 AND LEAST FOR CYLS 768-822.

(3) EQUIVALENT CIRCUIT.

8W28A

Figure 3-40. Head Select and Write Circuits

A multiple head select error may occur at any time, whether reading or writing. Multiple Head Select is sensed by the SCE/SCD circuit. If only one ground (or no ground) is sensed, the SCD voltage comparator output is +5v to indicate no error. Two or more grounds sensed through parallel dropping resistors causes the voltage comparator circuit to indicate the error. This generates a Current Fault; refer to Write Fault Detection for further information.

Write Data Processing

A Write operation actually begins before the voice coil positioner moves the heads to the desired track. The Transmit Head Address function code (Tag 7) gates the identifying number of the head to be used into the Head Address register (see Head Selection description). When the seek operation is completed, the unit generates an Interrupt signal. This places the unit logical number on the bus in lines when a Poll Devices tag is received. This signal informs the controller that the seek has been completed and the unit is on cylinder and ready to receive further commands.

The controller now sends a Request Status signal (Tag 4). After examining unit status, the controller sends an Interrupt Reset signal (Tag 9 BOB7) and continues its programmed operation. If conditions in the device permit, the controller responds to an Interrupt from the drive with an Operate function code (Tag 11) and Head Select (Bit 3), Read Gate (Bit 6), AM Search (Bit 1),and Data Enable (Bit 2). This enables the Read circuit logic to function with the selected head to search for an Address Mark and read a specific record address when a write record update is desired. The address is read from the Read Data line by the controller and compared with the address of the desired record. If the address is correct, the controller drops Read and brings up Write (Tag 11 BOB5). This disables the Read circuit and enables the Write circuit (Figure 3-41). Timing requirements of the Bus Out lines are a function of the controller and are specified in the controller manual.

Write data is transmitted to the unit and applied to a differential receiver. The write data is gated by a Write Gate signal enabled only when the drive logic indicates a safe write condition. The Gated Write Gate is generated when the following signals are true: On Cylinder, Not End of Cylinder, Write Command, Head Select and Not Write Protect. If Gated Write Gate is up, the data is allowed to pass through the remainder of the chain to the selected head and is written on the disk.

The output of the Write Toggle FF is processed by a symmetry restore circuit. This discrete component circuit (QEL) restores symmetry to the data signals that may have been lost in the write chain. Refer to the Logic Cards manual (see Preface) for a detailed description of this circuit.

The magnitude of the Write current flowing in the heads is controlled as a function of cylinder address (this is referred to as Write Current Zoning). These zones are divided into the following segments of tracks: 0-127, 128-255, 256-383, 384-511, 512-639, 640-767, and 768-822. Write current amplitude is reduced at each zone boundary from outer to inner tracks.

Two fault sensing circuits have been incorporated into the write circuits. One circuit senses the presence of any write current flowing in the heads. The other monitors the rate of current reversals being sent through the head. A lack of any current reversal for 900 nsec (nominal) when Write Gate is present, generates an AC Write Fault status. Both fault conditions signify an unsafe condition for writing and therefore disable the write driver as well as set Select Lock.

Read Data Processing

The read mode of operation is initiated by the application of Read Gate when the desired head is selected. Any flux transitions on the pack are then detected by the head and converted into an analog voltage. This analog signal (representing written data on the pack) is amplified and applied to the AGC Amplifier. A maximum of 30 μsec is required from the application of read data for the read chain to stabilize to the steady state amplitude levels.

AGC Amplitude Stage

The analog read data is applied to a low pass filter in the AGC amplifier stage (Figure 3-42). This filter attenuates the high unwanted frequencies (noise) in the read data signal and provides a linear phase response over the read data frequencies.

The output of the filter is applied to the AGC amplifier (A5306). The AGC amplifier provides a relatively constant output from a wide amplifier range on the input. This is accomplished by the AGC Control circuit which varies the gain of the AGC amplifier as the output varies.

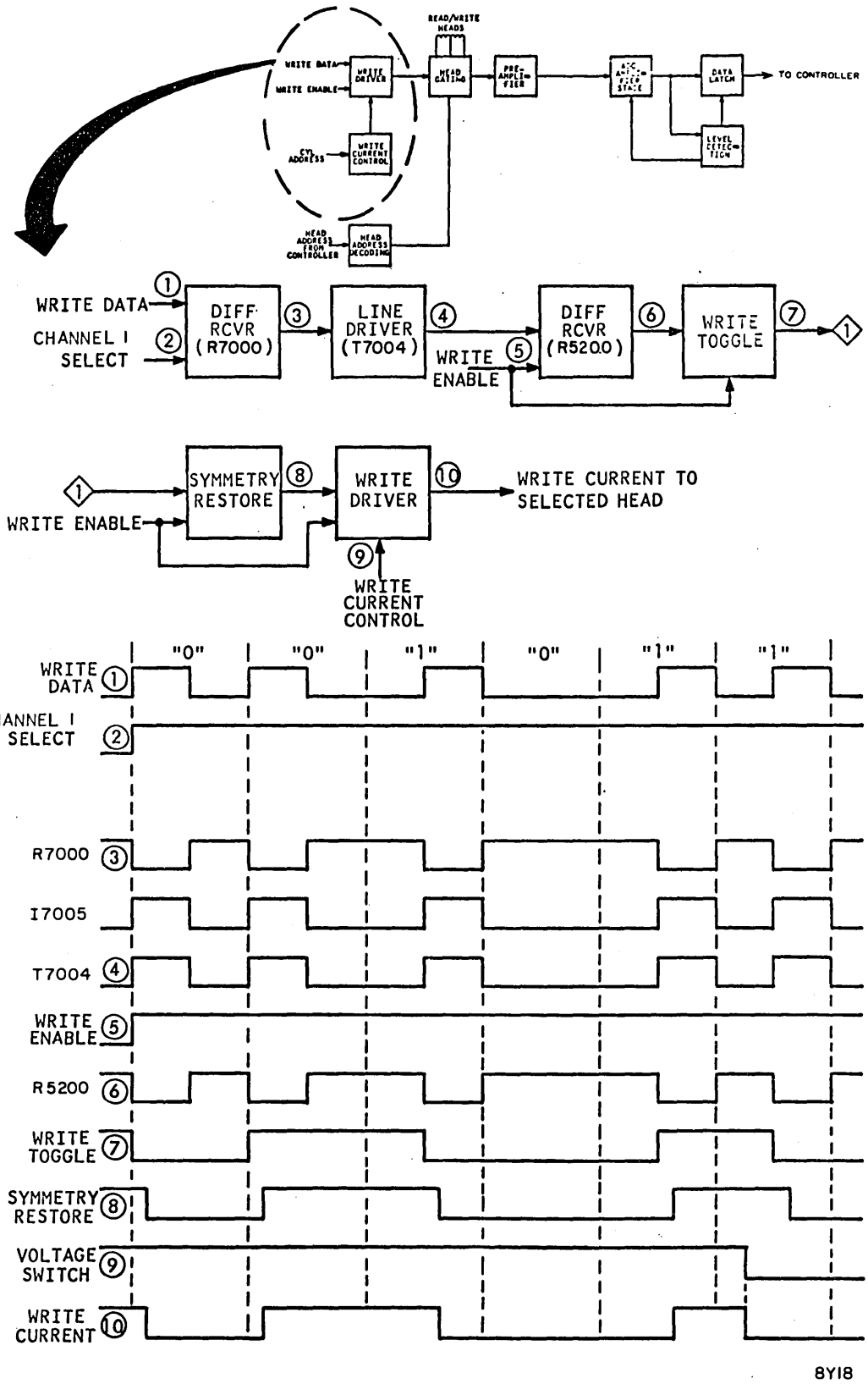


Figure 3-41. Write Chain Timing

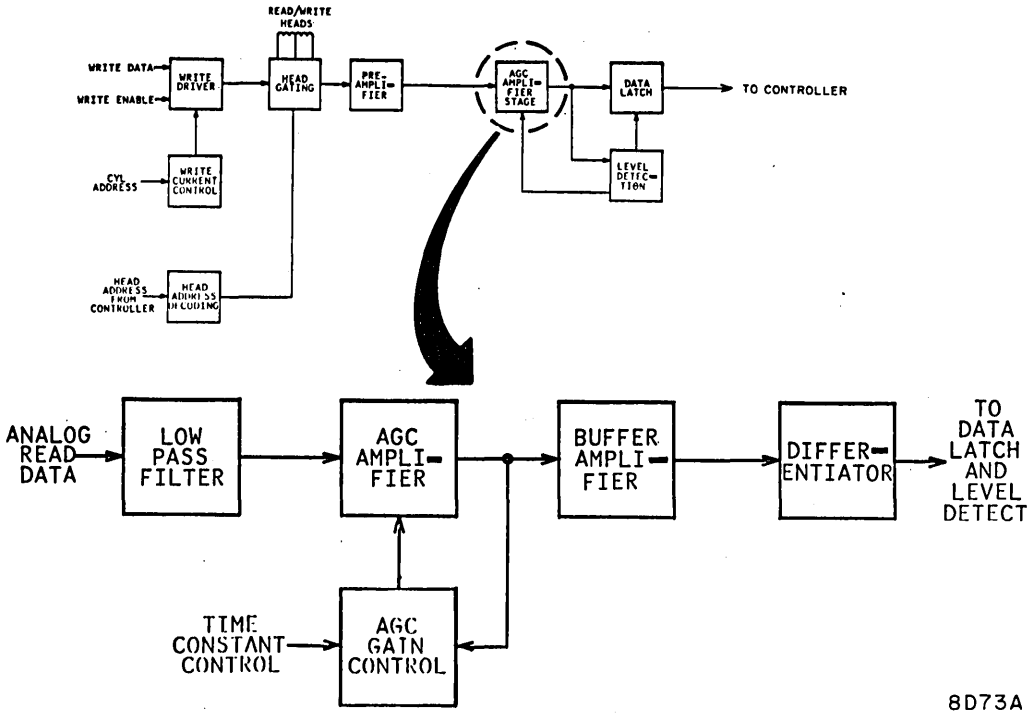


Figure 3-42. AGC Amplified Stage (Simplified Logic)

The output of the AGC amplifier is amplified and differentiated and then applied to the Data Latch and Level Detection circuits.

Level Detector and Time Constant Control

The Level Detector and Time Constant Control circuit contains an Amplitude Enable pulse generator, a data detector to detect the address mark gap, and a circuit to control the time constants of the AGC amplifier and level detector.

The output of the differentiator (Figure 3-43), is applied to a filter (A5400) which attenuates the third harmonic of the low frequency Read signal. This effectively lowers the resolution of the signal.

The output of the filter is amplified and then rectified. A capacitor is charged to the average dc level of the rectified signal. This voltage is then applied to the reference input of a comparator (A5402) and the rectified signal to the other input. When the rectified signal becomes more positive than the reference signal, the comparator switches. This produces a squarewave output that is used as an Amplitude Enable signal to reject noise and spurious pulses in the address gap area. The only time this output is used is during a Search Address Mark operation.

The Data Detector consists of a comparator (A5404) and a retriggerable single shot delay (X5402). The reference voltage on the comparator is a fixed dc voltage of about -0.46v. Each time the single voltage crosses the reference, the single shot is retriggered. The single shot will not time out as long as data above the fixed reference is being read. When a gap is reached, the single shot is retriggered by the last bit preceding the gap, times out for 670 nsec, then changes state to indicate an absence of data (Figure 3-43). The single shot is retriggered by the first data bit following the gap and by each succeeding bit, indicating that data is again present.

The Time Constant Control circuit switches the time constants of the AGC Amplifier and Level Detection circuits. Switching from a short time constant to a long time constant avoids responding to the loss of amplitude in the address mark gap area. Figure 3-44 shows block and timing diagrams of the Time Constant Control circuit with the address mark gap in three different positions.

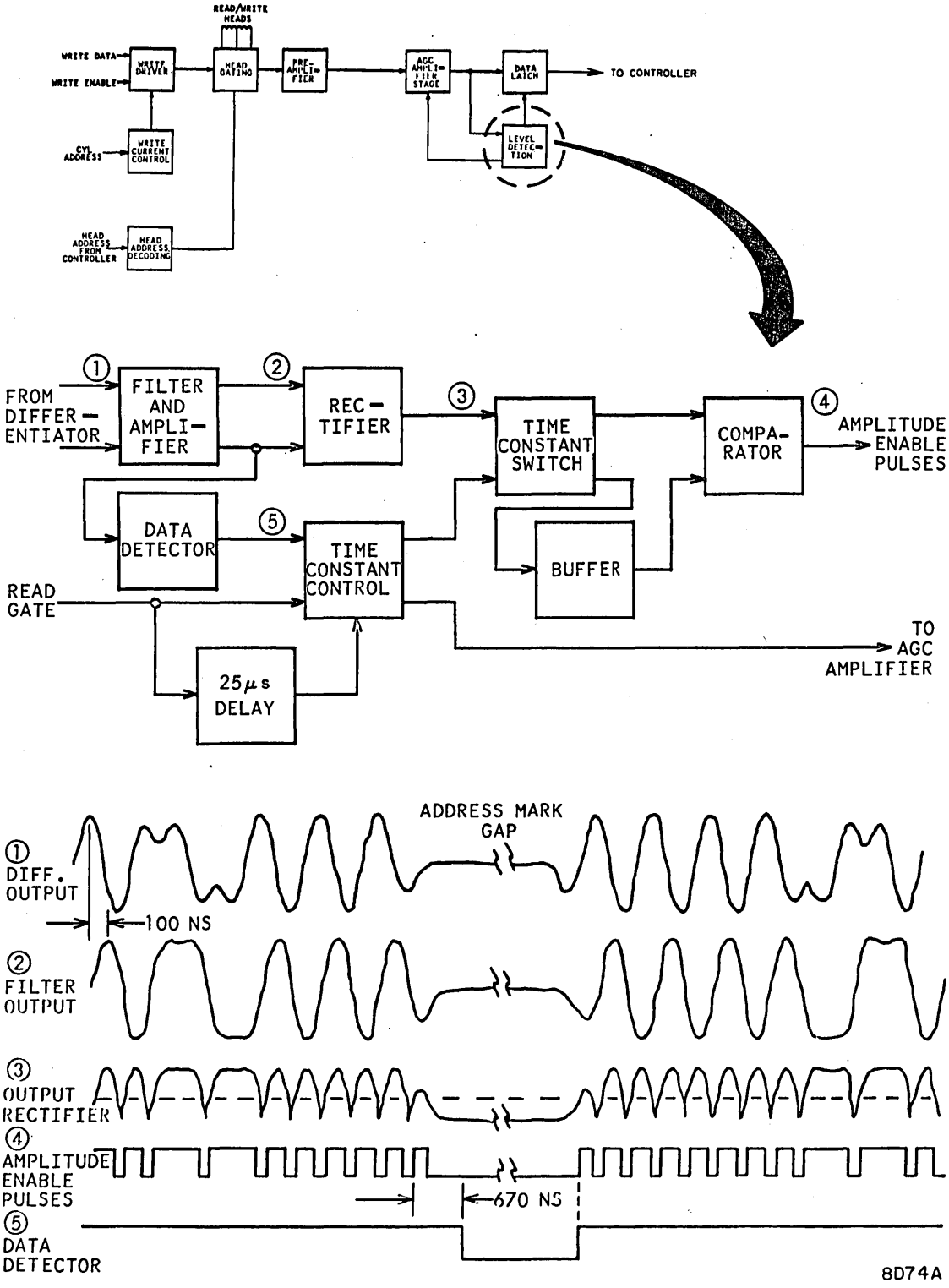


Figure 3-43. Level Detection Circuit

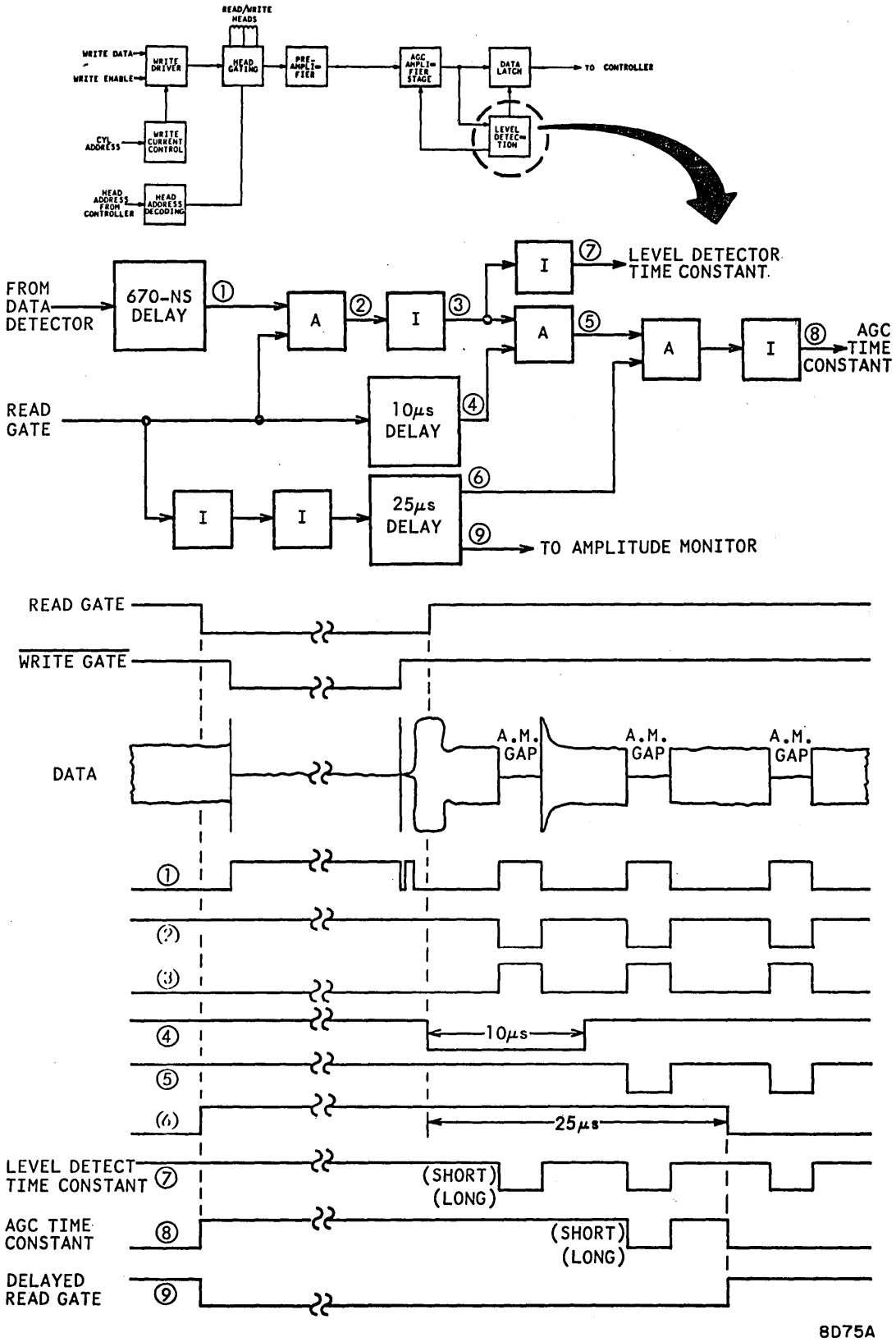


Figure 3-44. Time Constant Control Circuit

The Level Detector circuit is normally in a short time constant of 5 µsec in order to rapidly respond to changes in signal amplitude to maintain adequate margin in the amplitude enable function. The 5 µsec time is long enough so that the level detector does not respond to drop outs caused by disk surface bad spots. During the address mark gap, the level detector is switched to a time constant of 100 µsec. This prevents a shift in the comparator reference level so noise in the gap area does not produce false enable pulses.

The AGC amplifier is allowed 25 µsec to stabilize from the Head Select and Read Gate transients. A head may be selected and Read Gate can come up any time during a revolution of the disk, so it is possible that the address mark gap could occur during the 25-µsec stabilizing period. The AGC time constant is held in the short condition for the first 10 µsec following Read Gate. If a gap occurs between 10 and 25 µsec, the AGC amplifier is switched to a long time constant of 200 µsec to maintain a relatively constant gain level through the gap area.

Data Latch Circuit

The Data Latch circuit (Figure 3-45) consists of a low pass filter for the low resolution channel and zero-cross detectors and pulse generators for both the high and low resolution channels.

The Read Data from the differentiator is applied directly to the zero-cross detector in the high resolution channel and through the low pass filter to the zero-cross detector in the low resolution channel. As mentioned before, the filter lowers the resolution of the Read signal by attenuating the third harmonic of the signal.

The pulse generators (I5408 and I5410) produce pulses for each zero-crossing of the data. By appropriate delays, the low channel pulse (I5408) enables the K input to the output FF (K5403) in time for the high channel pulse (I5410) to clear it. A 50 nsec output pulse is formed when the delayed feedback resets the FF. The leading edge of the output pulse retains the timing of the high resolution channel. Note that the propagation time of the various gates must be considered to enable the K input at the proper time. Whenever the frequency of the read back data is decreasing, there is a camels hump in the differentiated output. (See Figure 3-43.) With sufficient frequency change and high resolution heads, the differentiated signal may actually pass through zero. The high resolution channel can react to these extraneous zero-crossing pulses; the low cannot because of the low pass filter. Therefore, they are ignored by the output FF because it cannot be cleared unless the low channel K enable is present.

The rejection of spurious pulses in the address mark gap is accomplished by ANDing the high channel pulses with an enable pulse. During the search mode, the Amplitude Enable pulses are passed through and ANDed with the high channel zero crossover pulses. When a zero crossover pulse corresponds to an enable pulse, it is passed through to reset the Output FF. There are noise created zero-crossover pulses in the address mark gap area. However, there are no enable pulses, so the reset input to the Output FF is disabled. Noise pulses in the low resolution channel are present at the set input of the FF, but are ignored because the FF is not reset during the gap period.

The Search Address Mark signal drops at the end of the gap. This applies a constant enable to the high resolution channel and all zero-cross pulses get through to the FF. This terminates the Amplitude Enable function and removes the Level Detector as a possible source of error during the actual reading of data.

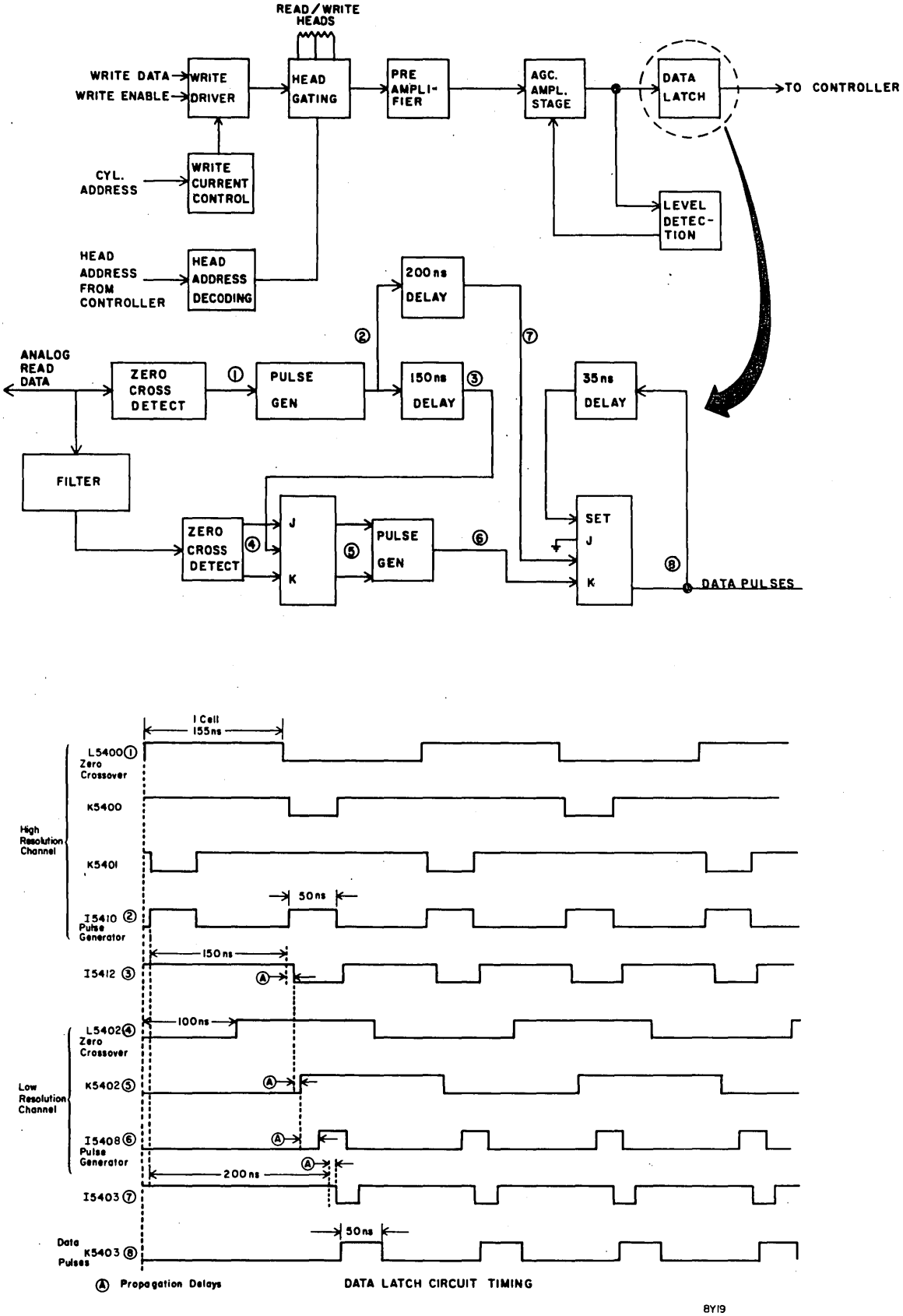


Figure 3-45. Data Latch Circuit

SECTION 4

KEY TO LOGIC

GENERAL

Section 4 contains information on logic symbology, operational amplifiers, integrated circuit package configuration, discrete component descriptions and logic card diagrams.

The logic used in this device consists of two styles of circuits: discrete component and integrated circuits. Discrete component circuits contain individually identifiable resistors, capacitors, transistors, etc.

Standard TTL logic levels used are: "1" = +3v and "0" = 0v. Standard ECL levels used are: "1" = -0.8v and "0" = -1.8v. All signals are named for their function when a "1". For non-standard logic levels or analog signal voltages, refer to applicable circuit description.

LOGIC CHASSIS

The Logic Chassis consists of the logic board wire wrap assembly and guiding piece parts for the logic cards.

Logic cards are plugged into the logic board wire wrap assembly. Guide rails connected to perpendicular panels guide the cards into place and restrict horizontal or vertical movement.

Wire wrap pins extend through the back panel. The logic cards mate with these pins on one side of the back panel. On the other side, the "wire wrap" side, wiring interconnects the logic functions between cards. This wiring is secured to the pins by the wire wrap technique. These pins also provide convenient test points for monitoring logic levels of all signals entering and leaving each card.

The wire wrap surface of the logic board wire wrap assembly contains wire wrap pin identification (Figure 4-1). Logic cards are designated by horizontal row (A) and vertical column (1 through 16). Wire wrap pins are then called out by pin number and column A or B. For example, A8-12B is the back panel pin at logic row A, position 8, pin 12 of column B.

JA01 through JA04, PA1, PA2, PA6, PA7, P09, and JA10 are auxiliary connectors used to interface logic cards with maintenance panel, I/O connectors, etc. Pin identification is by pin number (1 through 14) and row (A or B). (JA01-5A is auxiliary connector JA01, pin 5, row A.)

LOGIC CARDS

PHYSICAL DESCRIPTION

All components of the logic cards (Figure 4-2) are mounted on one side of a printed circuit board (PCB). Numeral designators (1 through 99) are etched on the non-component side of the board identify each transistor. A 4-character alphanumeric designator is etched on the non-component side of the board to identify the card type. A matrix code (alphanumeric) also appears on this side. Non-amplifying components such as integrated circuits, resistors, capacitors, diodes, etc., are not marked.

PIN ASSIGNMENTS

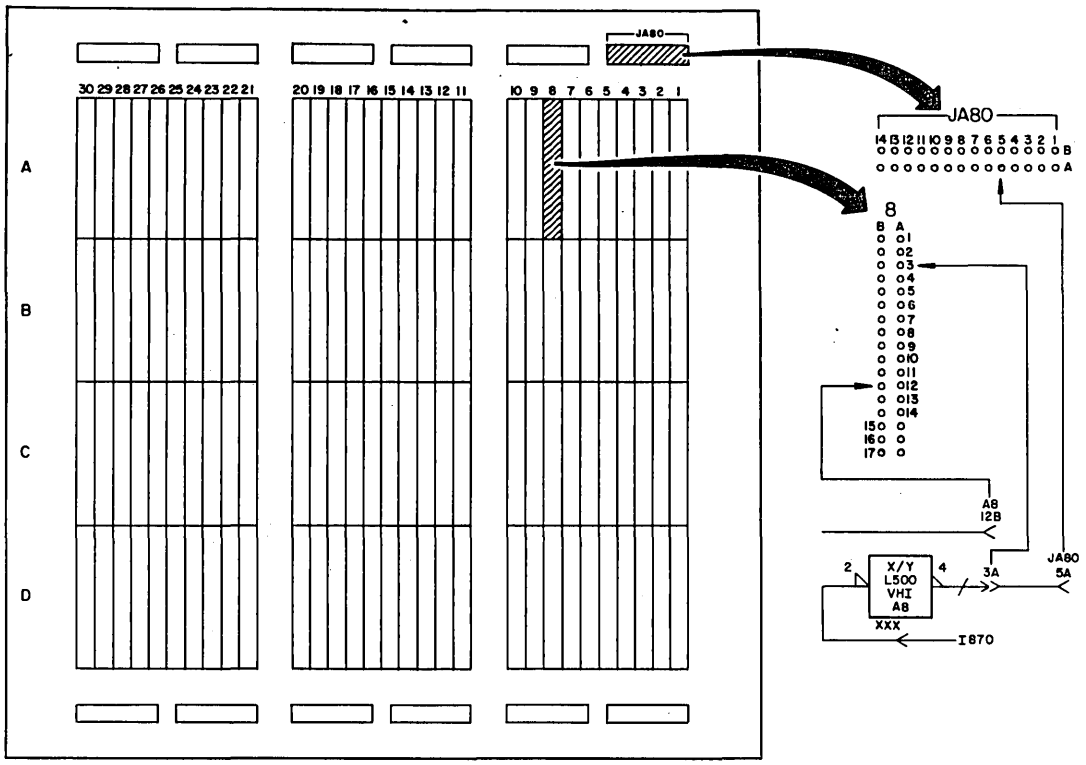
Cards are equipped with a 62-pin (sockets) connector. Connectors are mounted along the shorter dimension on the component side of the board.

The pins of each card connector are arranged in two columns (A and B) and are numbered from the top starting with pin 1 and continuing through pin 14 on the half-size card. The pins of the full-size card are numbered 1 through 34, however, pins 18A, 18B, 19A, 19B, 20A, and 20B are omitted.

The logic chassis wire wrap surface (side opposite surface where cards are installed) contains wire wrap pin identification information adjacent to each chassis row. Wire wrap pins are numbered 1 through 17 in each chassis row. When a full-size card (spans two logic rows) is installed in the logic chassis, card connector pins (sockets) 1A and 1B mate with wire wrap pins 1A and 1B of the upper row, while card connector pins 21A and 21B mate with wire wrap pins 1A and 1B of the row immediately below. The logic diagrams for this unit show connections in terms of wire wrap pins.

TEST POINTS

Test points are located near the edge of the card opposite the connector and in other strategic places on the component side of the board. Test points are identified alphanumerically starting with A on the top,outer edge. Test points A and Z are available for ground reference on full-size cards. Only test point Z is available for ground reference on half-size cards.



Wire Wrap Pin Identification

A8	Position 8 in Chassis Row A
12B	Pin number 12 in Column B
3A	Pin number 3 in Column A. When Chassis Row and Position are not listed it is identical to the one above it.
JA80	Auxiliary connector used to input or output signals to/ from Back Panel.
5A	Pin number 5 in Row A

Logic Representation

X/Y	Function symbol
L500	Logic term or identifier
VHI	Circuit type designator. Alpha characters indicate discrete component circuits, numeric characters indicate integrated circuits.
A8	Location of Logic Card. Connector 8 of Row A. Location of full size cards identified with top connector.
xxx	Special circuit characteristics. (Oscillator frequency, delay period, etc.).
2	Input applied to transistor Q2.
4	Output transistor (if applicable) Q4.
—/—	non Logic Level
≫,<	Pin connections.
—<	Indicates direction of signal flow.
-1870	When no pin connections are indicated, it is a continuous foil going from preceding term to indicated term.

8Y36

Figure 4-1. Wire Wrap Board Assembly

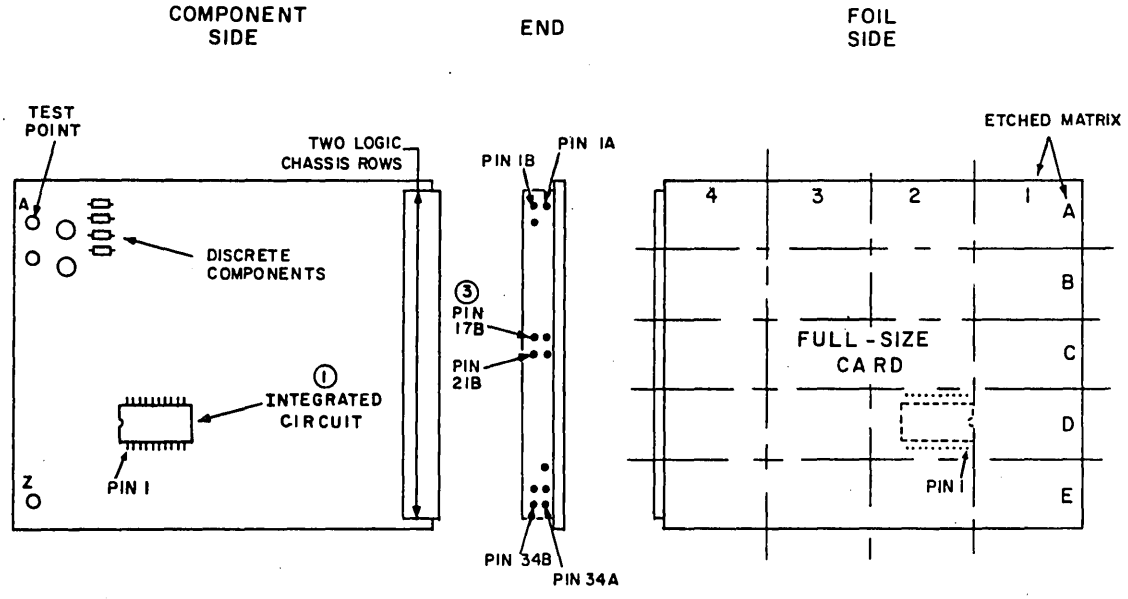


Figure 4-2. Logic Card Detail

LOGIC SYMBOLOGY

INPUT/OUTPUT STATE INDICATORS

There are two input/output state indicators used in this manual set. They are the polarity indicator (—▷| or |▷—) and the logic negation indicator (—○| or |○—).

The input polarity indicator indicates the most negative potential is required to satisfy the logic function represented by the qualifying symbol. The output polarity indicator indicates the most negative potential is present at the output when the logic function is satisfied. The absence of the polarity indicator indicates the most positive potential is present.

The presence or absence of the logic negation indicator tells the conditions that are necessary to satisfy the function of the logic symbol. The presence of the circle indicates a "0" logic level on that line is needed to satisfy the function. The absence of the circle indicates a logical "1" is needed to satisfy the function.

The input/output state indicator depicts the occurrence of inversion. Figure 4-3 shows some representative examples of the polarity indicator being used in this manner.

DYNAMIC INDICATOR

The presence of a dynamic indicator (▷) just inside a symbol indicates the inputs are gated (satisfied) with the dynamic positive-going transition of the input line to the state shown. A logic negation indicator (circle) accompanying the dynamic indicator signifies that a negative-going transition is required to gate in the inputs. Absence of the dynamic indicator indicates the inputs are gated (satisfied) with the static state of the input line.

SIGNAL LINE INDICATORS

Non-Standard Levels

Some signal line indicators indicate non-standard levels on input/output lines. These signal line indicators are as follows:

—/— non-standard logic levels
—X— analog or non-logic levels
—ƒ— variable control

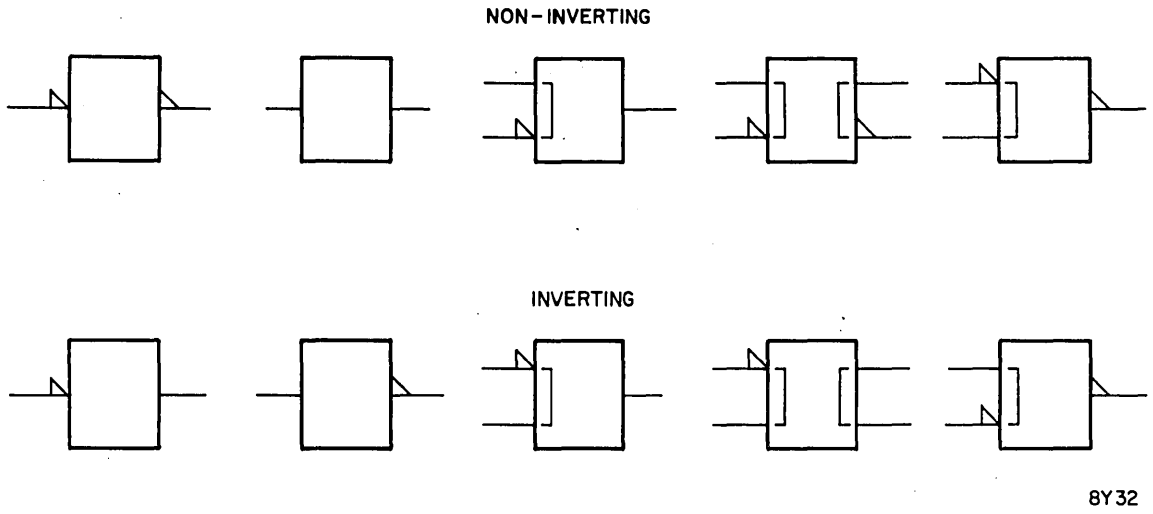
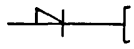


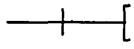
Figure 4-3. Inversion Conventions

Absence of these indicators shown above indicates a standard logic level.

Inhibit

The inhibit line indicates gating of the logic function will be inhibited whenever the line is at the level indicated by the input state indicator. Inhibit line symbols are as follows:


with polarity indicator


without polarity indicator

Miscellaneous

Other signal line indicators are as follows:

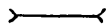
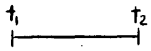
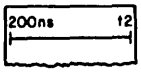
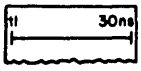
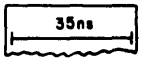

test point


twisted pair

FUNCTION SYMBOLS

Circuit function symbols for discrete components and integrated circuits are as follows:

1	OR gate or inverter
&	AND gate
=1	exclusive OR
▷	amplifier (with or without gain)
▷	amplifier with adjustable gain
Σ▷	summing amplifier
∫▷	integrating amplifier
∂▷	differentiating amplifier
X/▷	digital to analog conversion
X/▷	digital to analog conversion with adjustable gain
▷/Y	analog to digital conversion
▷X/Y	amplifying level translator (gain noted outside box)
|▷|	positive analog rectifier (symbol preceded by a minus sign if negative rectification is used)
ΣX/▷	analog summation of digital inputs. Reference voltage outside box indicates output signal level resulting when specified input(s) are negated
▷⊓Y	Schmitt trigger

	saturable,non-linear,gain controlled amplifier
F▷	function generator
∩▷	active bandpass filter
⌐∩	bandpass or resonant circuit
	bidirectional switch
X/Y	Level conversion - transmission line to logic level, switch state (ground or open) to logic level, logic level to power output (to drive lamp, relay, solenoid, etc.)
1 	retriggerable multivibrator (single shot)
	symmetry restoration circuit
	ones delay - when input changes to a "1" a 200 nsec delay occurs before the "1" is passed on
	zeros delay - when input changes to a "0" a 30 nsec delay occurs before the "0" is passed on
	both transitions are delayed by 35 nsec

INPUT/OUTPUT DESIGNATORS

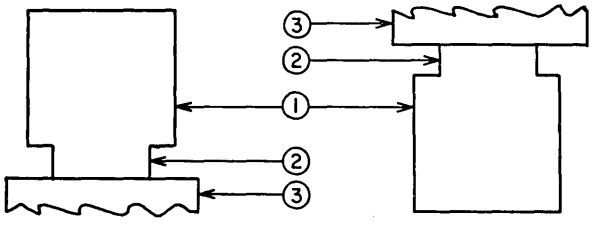
Inputs are individually identified as necessary by an input designator inside the symbol block and adjacent to the left side following all prefixes indicating dependency. These input designators follow:

R	reset or clear
S	set
G	gating type input that affects other inputs or outputs
J	J input of J-K flip-flop
K	K input of J-K flip-flop
Z	used to link gating (clock) input of control block to J and K inputs of J-K flip-flops
T	toggle or complement input
D	data input of D-type flip-flops
C	a gating (clock input for D-type flip-flops)
→	shift right (or down)
←	shift left (or up)
+1	increase contents by one (count up)
-1	decrease contents by one (count down)
]OR[	indicates grouped inputs that maintain a fixed relationship in states and always change together
1, 2, 4, 8	indicates relative weighting of inputs or outputs in codes. They may be consecutive, binary,decimal representation of binary values,etc.
A, B, C, ETC.	when two or more of these are used together in inputs to a symbol, it indicates individual signals or individual groups of signals to be identified for further operations such as arithmetic functions

Certain input designators (C and G) may also be used as prefixes to other input designators, but not to each other, C and G indicate dependency of every designator, such as D,they prefix, and are referred to as dependency notation. For example, CD indicates that the input is gated to a D-type flip-flop only when the C input is active. Gate dependent inputs (G) may be distinguished from each other by 1, 2, etc., following the G. Where more than a single G term is involved, commas are used to separate the numbers. Clock dependent inputs for loading data are denoted by a "C". Different C inputs are distinguished by a number following the C.

COMMON CONTROL BLOCK

Signals entering the common control block (Figure 4-4) are common to more than one



① COMMON CONTROL BLOCK

② NECK

③ SECTION(S) CONTROLLED BY COMMON CONTROL BLOCK.

8Y33

Figure 4-4. Common Control Block

section of the circuit. The neck of the common control block abuts the top or bottom of the sections it controls. Input designators may include C, G, R, →, ←, +1, -1, plus select lines with or without decoding.

WIRED FUNCTIONS

The logic representation for wired functions is shown in Figure 4-5. These functions are used where circuits have the capability of being combined as an OR function by having the outputs connected. This is simply a physical connection and no electrical or electronic components are involved. The logical interpretation of a wired OR function simply requires that one of the inputs be a logic "0" before the output can be a logic "0". The wired AND output will be a logic "1" only when both inputs are logic "1's".

INTEGRATED CIRCUITS

Figure 4-6 shows the schematic version (as shown on card schematic diagram) and the logical representation (as shown on logic diagrams) for the same representative integrated circuit.

Referring to Figure 4-6 it is apparent that the two versions are essentially the same. Both views identify pin numbers, the function symbol, and the CDC element number for the circuit. Refer to Section 5 for manufacturer's information on the various element numbers.

The last item of information regarding these two representations involves the location code which borrows part of the schematic symbols reference designator. In the reference designator (U-A4B), the U specifies a non-amplifying integrated circuit, the A4 is the circuits board matrix location for the package, and the B indicates the section of the package. (A 140 package is a four section package. Each section is a separate circuit. Sections are identified A through D.) The location code (on logic drawings) borrows the matrix location and additionally specifies the location of the card in the logic chassis: position 5.

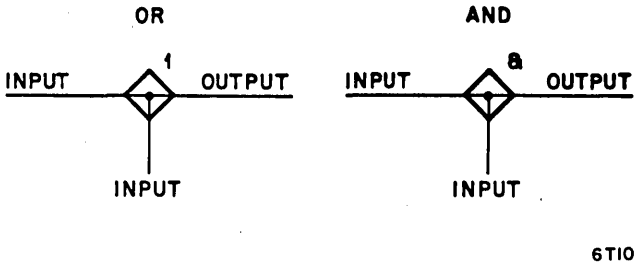


Figure 4-5. Wired Functions

OPERATIONAL AMPLIFIERS

INTRODUCTION

The operational amplifier (op amp) is a high-gain integrated circuit that can amplify signals ranging in frequency from dc to its upper frequency limit, which may be more than one megahertz. It is used extensively in the drive as a linear amplifier of servo analog signals. Because of its versatility, however, it has multiple applications.

The op amp approaches the following characteristics of an ideal amplifier:

1. Infinite voltage gain
2. Infinite input resistance
3. Zero output resistance
4. Zero offset: output is zero when input is zero
5. High bandwidth frequency response

BASIC CIRCUIT ELEMENTS

Figure 4-7 is a highly simplified schematic of a typical op amp with its basic feedback network. Detailed circuit analysis information may be obtained by referring to the manuals prepared by the applicable manufacturers.

INPUT STAGE

All op amps utilize a differential amplifier in the input stage. This circuit may be relatively simple, as shown, or may consist of multiple circuits with FTEs or Darlington-connected transistors. The advantage of this type of amplifier is that it amplifies the difference between the two input signals. For example, if 10 mv are applied to the non-inverting input while 9 mv are applied to the inverting input the extra 1 mv difference is amplified. The amplification,which may be a voltage gain of up to 100,000 is linear until the op amp saturates or until increasing frequency causes rolloff.

If the same input is applied to both input terminals, the signal is referred to as the "common-mode" input signal. In the preceding example, the 9 mv are the common-mode input, while 1 mv is the differential input. In the ideal op amp, the output is zero with

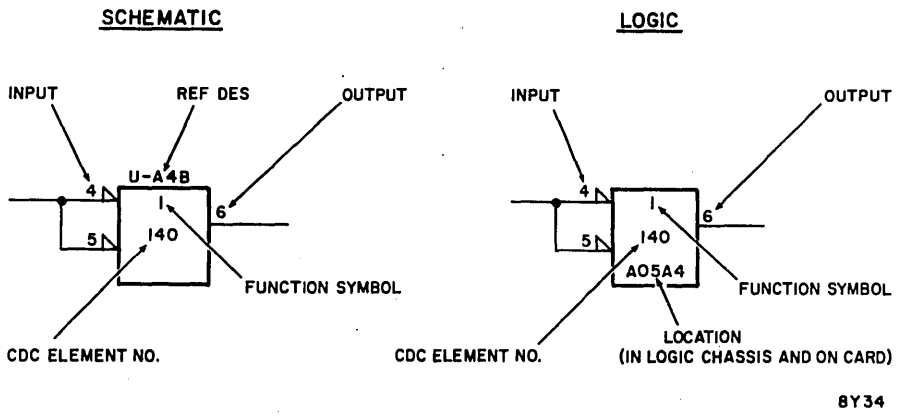


Figure 4-6. Integrated Circuit

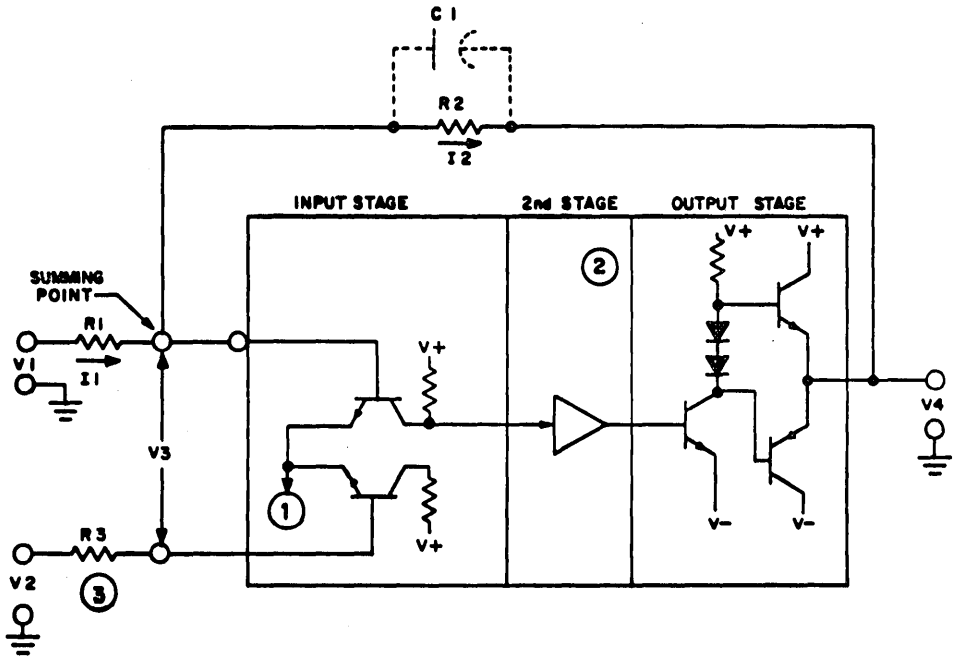


Figure 4-7. Simplified Op Amp Schematic

identical inputs. Only the difference (1 mv) is amplified. Since the common-mode input is not amplified, signals common to both, such as noise and hum, are cancelled.

SECOND STAGE

Not all op amps have a second stage. If used, however, it may contain additional amplification and level shifting.

BASIC CIRCUIT FUNCTIONS

Resistors R1 and R2 provide degenerative feedback to control the overall gain of the circuit. As long as the ratio R2/R1 is low compared to the open loop gain at the operating frequency, circuit gain is independent of the characteristics of the specific op amp.

Rapid analysis of this circuit is possible if two basic principles of op amps are assumed:

1. Insignificant current flows into either input terminal; it can be assumed to be zero.

2. The differential voltage (V3) is insignificant and can be assumed to be zero.

Rule #1 may be presumed since the input impedance is very high. As a result, all current (I1) entering the summing point must leave it (I2). These currents are:

$I1 = V1/R1$

$I2 = -V4/R2$

The minus (-V4) indicates that the output is the inversion of the input. Since no current flows into the op amp, I1 must be equal to I2. By Ohms Law:

$V4/V1 = -R2/R1$ or $V4 = -V1(R2/R1)$

Therefore, the output is simply the ratio of R2/R1. This linear output/input relationship holds true as long as the input (V1) is not of sufficient amplitude to saturate the op amp.

Resistor R2 is frequently shunted by a capacitor. This controls the roll-off characteristics of the circuit where the full op amp bandwidth is not required. The effective feedback to the input is the resistance of R2 in parallel with the capacitive reactance of C1. Capacitive reactance decreases as frequency increases. Therefore, a frequency increases, the effective impedance of R2-C1 decreases to reduce overall gain.

If C1 is large enough, its charging time becomes more of a factor. The output cannot react as fast as the input may change. This is the integrating or low pass function. For example, doubling the frequency halves the gain. The output is the mathematical integral of the input when the effects of C1 predominate over the effects of R2. Thus, if the input voltage is proportional to velocity, the output is proportional to distance.

Since there is actually a slight current (measured in nanoamperes) entering the differential stage, the difference or unbalance between the two input currents would be amplified. This results in an error known as dc offset, that is, the output would be non-zero with a zero common-mode input. If, however, the currents are made to be equal, that is, they see equal input impedances, they are common-mode and are cancelled. Resistor R3 is selected to balance out the offset voltage and current by making the impedance to ground of the two inputs equal.

Rule #2 holds true as long as feedback is provided by R2 or its equivalent. As long as the amplifier is not saturated, it will adjust its output voltage to maintain the differential voltage V3 at zero. Therefore, the summing point is at V2. Since V2 is usually at ground potential, the summing point is also at ground. This is a "virtual" ground, that is, it is at ground potential even though there is no connection between this point and true ground. If the summing point is monitored with an oscilloscope, little or no signal can be observed.

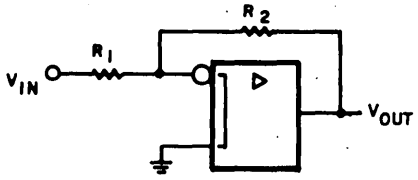
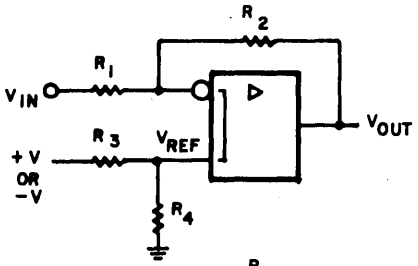
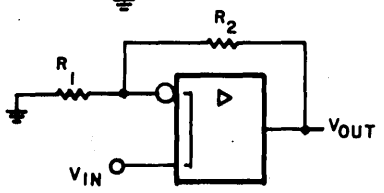
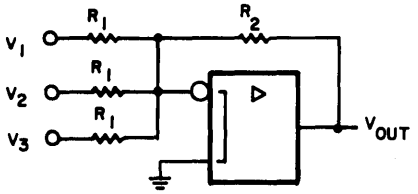
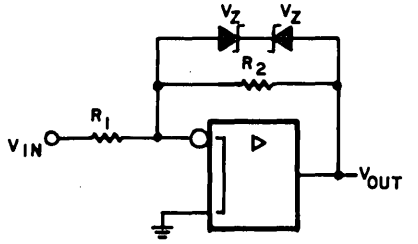
Typical op amp circuit functions are illustrated in Figure 4-8.

SCHMITT TRIGGER CIRCUITS

Operational amplifiers can also be connected in the Schmitt trigger configuration (Figure 4-9). Note that the degenerative feedback path is not provided. It is replaced by a regenerative feedback path. This is the open loop configuration: if the voltage at the non-inverting input is greater than the voltage at the inverting input, the output is saturated at its most positive value. Reversing the inputs causes the circuit to slew (change) at its maximum possible rate to saturate negatively.

All Schmitt triggers have hysteresis. Hysteresis is supplied by regenerative feedback from the output to the non-inverting input.

Consider A376 of Figure 4-9. Assume the voltage at A is zero. A voltage divider network (not shown) sets point B at +1.28v.

CIRCUIT TYPE	SYMBOL	OUTPUT ①
INVERTING AMP		$V_{OUT} = -\frac{R_2}{R_1} V_{IN}$
INVERTING AMP WITH REFERENCE VOLTAGE		$V_{OUT} = V_{REF} + \frac{R_2 (V_{REF} - V_{IN})}{R_1}$ OBSERVE ALGEBRAIC SIGNS IF COMPUTING $V_{OUT} = 0$ IF $V_{IN} = V_{REF}$ $V_{REF} = \pm V\left(\frac{R_3}{R_3 + R_4}\right)$
NON INVERTING AMPLIFIER		$V_{OUT} = \frac{V_{IN} (R_1 + R_2)}{R_1}$
SUMMING AMPLIFIER		$V_{OUT} = -\left[\frac{R_2}{R_1} (V_1 + V_2 + V_3)\right]$
INVERTING AMPLIFIER WITH OUTPUT LIMITING		$V_{OUT} = -\frac{R_2}{R_1} V_{IN}$ IF $\pm V_{OUT} \leq V_Z$

NOTE:

① MINUS SIGN (-) INDICATES THAT OUTPUT IS INVERTED.

7J91-1

Figure 4-8. Op Amp Circuit Functions (Sheet 1 of 3)

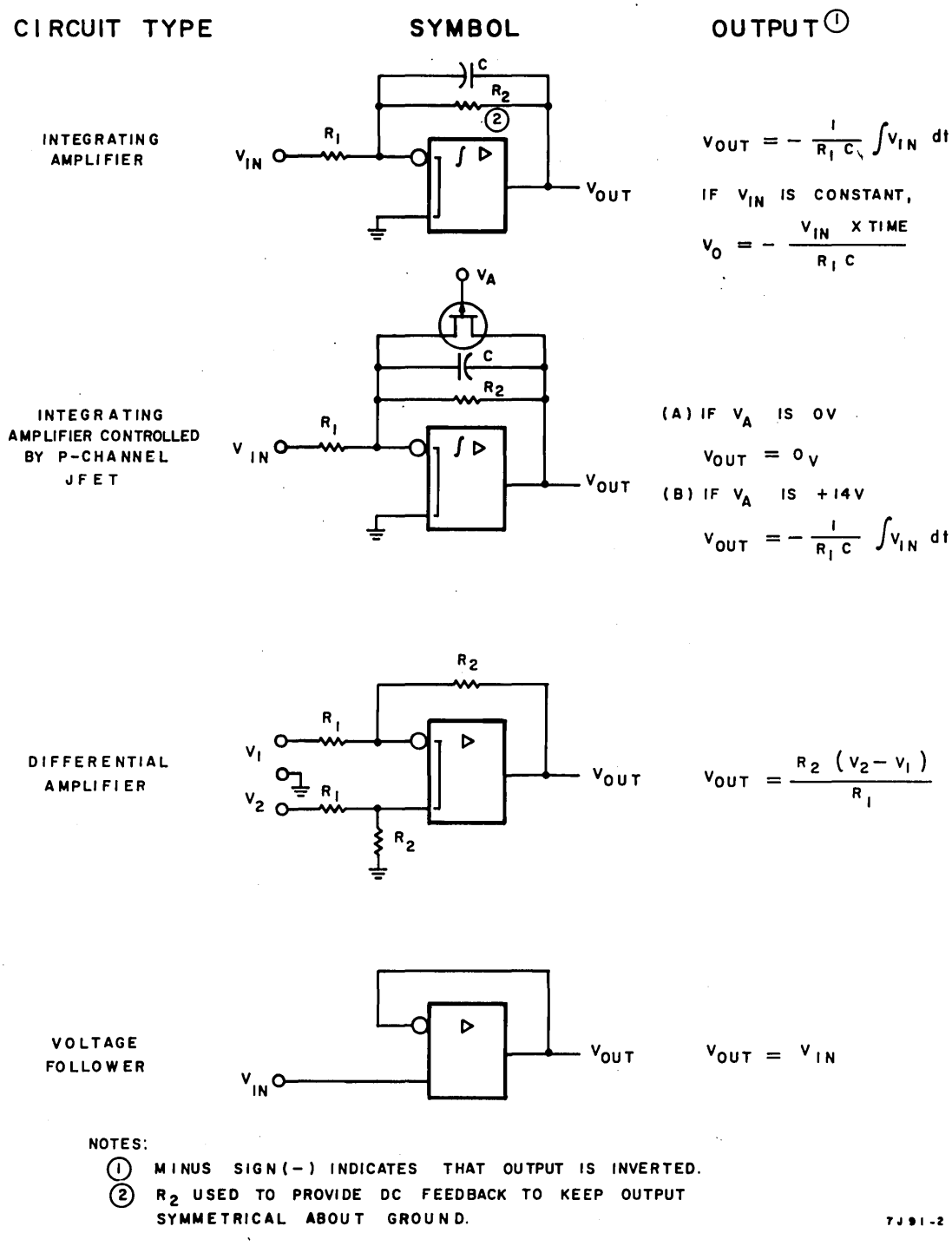


Figure 4-8. Op Amp Circuit Functions (Sheet 2 of 3)

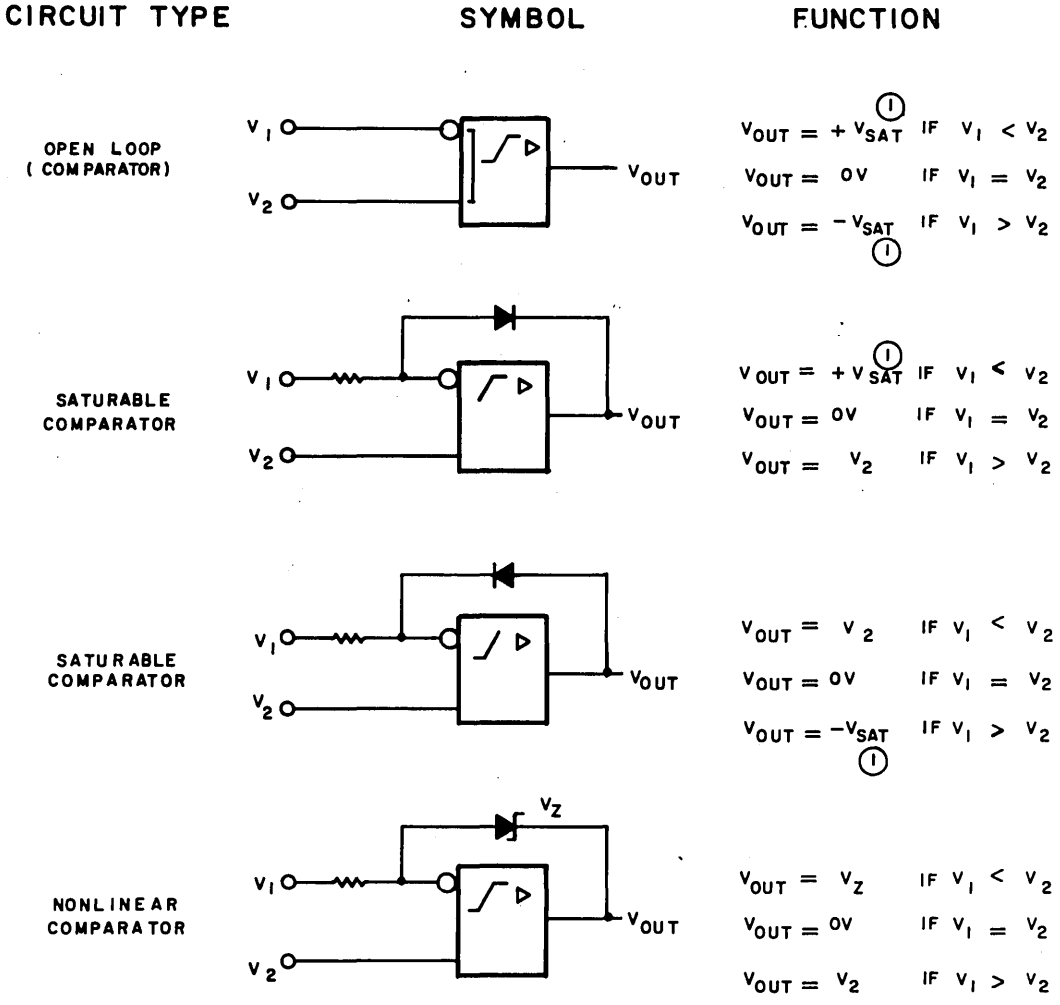


Figure 4-8. Op Amp Circuit Functions (Sheet 3 of 3)

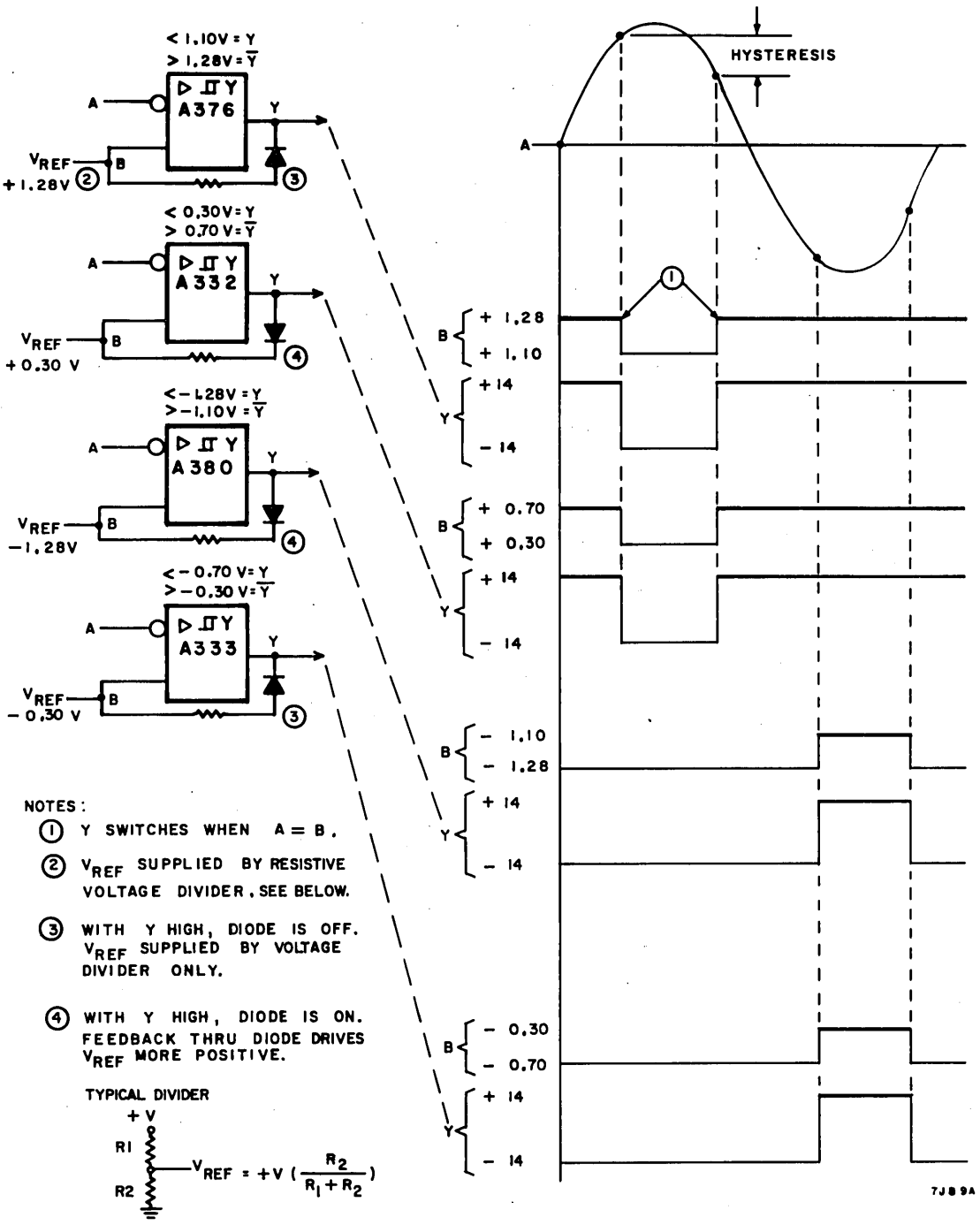


Figure 4-9. Op Amp used as a Schmitt Trigger

Without feedback and, since the non-inverting input is more positive than the inverting input, the output is saturated positively.

As the input A goes more positive, the output does not change until A equals B (+1.28v). The differential voltage is then zero, so the output starts to switch to a zero-volt output. However, there is now a path from Y to B; the B input becomes less positive than the A input. The output very quickly saturates negatively.

With about -14v available at Y, the voltage at B is reduced to +1.10v. The input must now swing to less than +1.10v for the output to change its state back to positive saturation.

The remaining circuits work in a similar manner.

DISCRETE COMPONENT CIRCUITS

Figure 4-10 shows a schematic (as shown on card schematic diagram) and the logical representation (as shown on logic diagrams) for the same theoretical discrete component circuit. Three lines of information are contained within the logic symbol. The top line is the function symbol and designates the board logic function of that particular symbol. In this case, ▷ represents an amplifier, the logic function performed by the circuit. The second line, also an alphabetic code, designates the circuit type being used (HAB). The circuit type is a subdivision of the function identifier (specifically a high level amplifier). By using the circuit type designator, detailed information on that particular circuit may be obtained by referring to Section 6.

The third line within the symbol identifies which logic card location and circuit is located on.

The numbers on the input lines to the symbol indicate which transistor is driven by that input line. For example, the upper input has a number 22 on its line, showing that it drives transistor number 22 (i.e., Q22 on the card schematic diagram).

The output lines also have numbers associated with them. These numbers indicate which transistor directly feeds the output line. For example, the lower output line has a number 40 above it, indicating that the output from transistor number 40 (Q40 on the card schematic diagram) drives the lower output line.

The lines on the interior of the logic block that bracket both inputs and both outputs

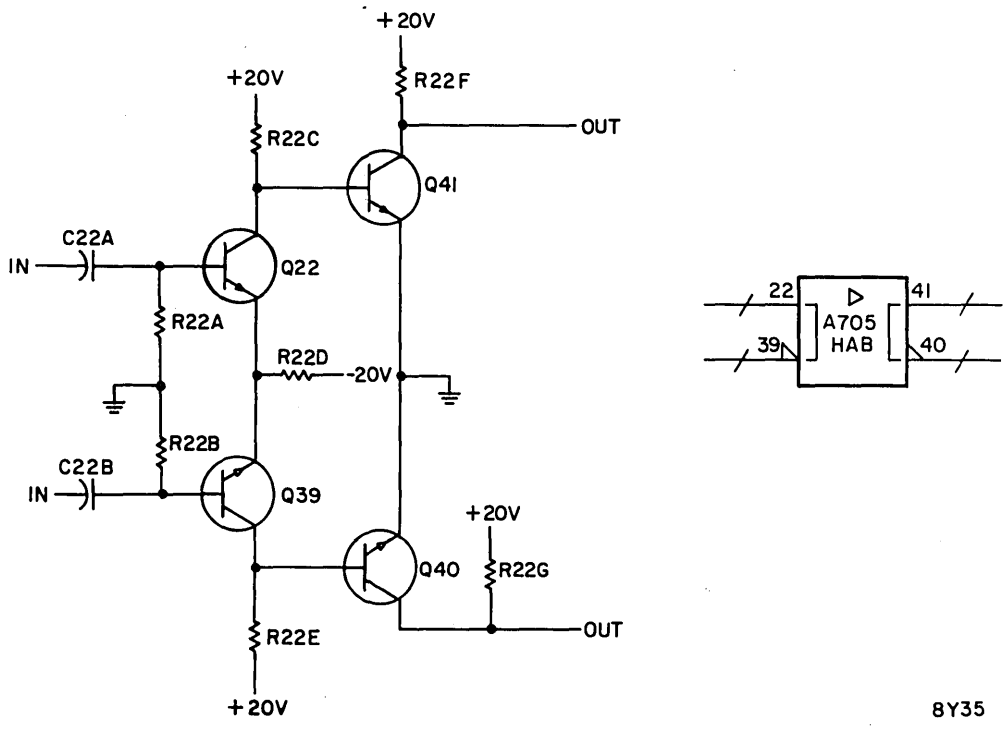


Figure 4-10. Discrete Component Circuit

show that the input lines and the output lines are differentials. The relative level indicators show that the amplifier does not invert the signal. Slashes on the inputs and outputs show that the signal levels are non-standard.

For schematic diagrams of discrete component circuits used in this device see Section 6. An analysis of circuit operation supports each circuit diagram. The order of presentation is in accordance with the three-letter alphabetical circuit type designator.

SECTION 5

INTEGRATED CIRCUITS

DESCRIPTION

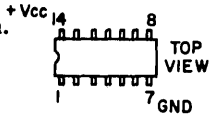
The 140 circuit is a two input-one output active low level output AND/NAND gate.

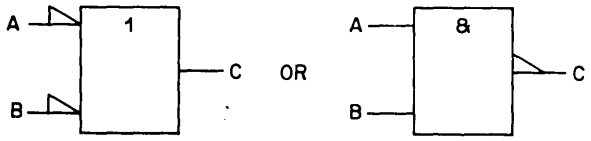
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 140 manufactured by Fairchild Semiconductors (P/N 9002) used for low speed applications.
4. Type 140S manufactured by Texas Instruments (P/N 74S00) used for high speed applications.
5. Propagation delay time:

Type	Delay Time (NSec)
140	18
140H	10
140S	5

6. Package pin configuration.

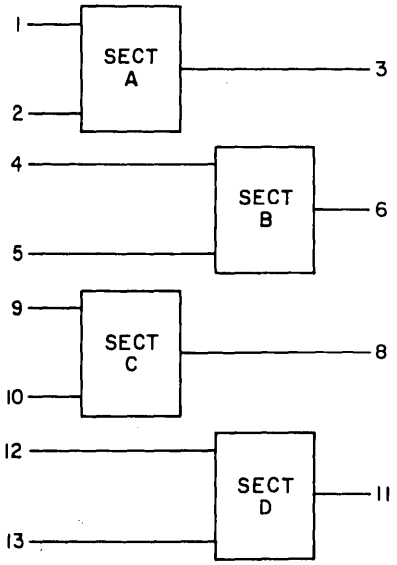




LOGIC SYMBOL

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

TRUTH TABLE
(FOR ONE GATE)



PIN ASSIGNMENTS

Description

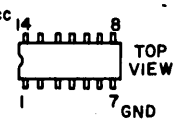
The 141 circuit is a three input-one output active low level output AND/NAND gate.

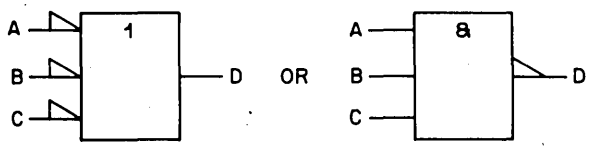
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 141 manufactured by Farichild Semiconductors (P/N 9003).
4. Type 141H manufactured by Texas Instruments (P/N SN 74H10).
5. Type 141S manufactured by Texas Instruments (P/N SN 74S10).
6. Propagation delay times:

Type	Delay Time (NSec)
141	10
141H	6
141S	3

7. Package pin configuration.

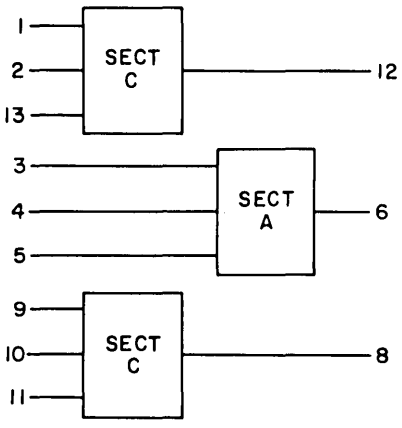




LOGIC SYMBOL

A	B	C	D
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

TRUTH TABLE



PIN ASSIGNMENTS

Element 141 Sheet 1 of 1

Description

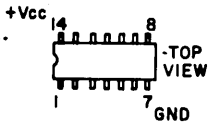
The 143 circuit is a four input-one output active low level output AND/NAND gate.

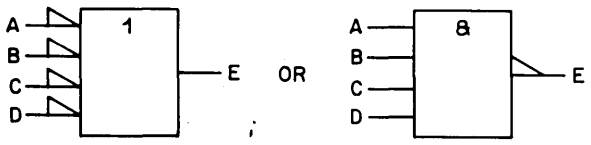
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 143 manufactured by Fairchild Semiconductors (P/N 9009).
4. Type 143H manufactured by Texas Instruments (P/N SN 74H40).
5. Type 143S manufactured by Texas Instruments (P/N SN 74S40).
6. Propagation delay time:

Type	Delay Time (NSec)
143	10
143H	6
143S	3

7. Package pin configuration.

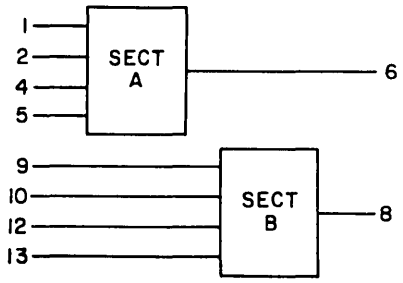




LOGIC SYMBOL

A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	1
1	1	1	1	0

TRUTH TABLE
(FOR ONE GATE)



PIN ASSIGNMENTS

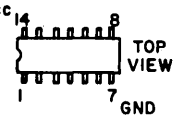
Description

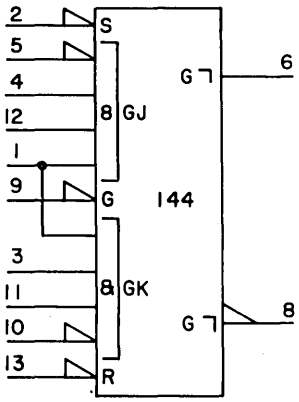
The 144 circuit is a JK Flip-flop capable of synchronous or asynchronous input operation. The asynchronous inputs control the state of the flip-flop independent of static conditions of the clock and synchronous inputs. With pin 13 or pin 2 LOW one output will be high, but if opposing data is present at the synchronous inputs and the flip-flop is clocked, the low output may momentarily spike HIGH synchronous with a positive transition of the clock. A low level to the set input (pin 2) will set pin 6 to high level regardless of the level at the clock (pin 9) input. A low level to the reset (pin 13) input will clear pin 6 to low level regardless of the level of the clock input.

Data is accepted by the master while the clock is in the low state. Transfer from the master to the slave occurs on the LOW to HIGH transition of the clock. When the clock is HIGH, the J and K inputs are inhibited.

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 144 manufactured by Fairchild Semiconductors (P/N 9001).
3. Package pin configuration.





GJ-J OUTPUT CONDITIONED BY LEADING EDGE OF DYNAMIC TOGGLE(G)

GK-K OUTPUT CONDITIONED BY LEADING EDGE OF DYNAMIC TOGGLE(G)

G-GATE INPUT, HAS NO DIRECT EFFECT ON CIRCUIT, BUT MUST PRESENT BEFORE SIGNALS PRESENT ON INPUT(S) CAN BE TRANSFERRED TO OUTPUT(S)

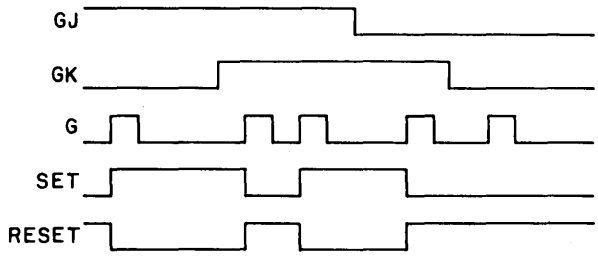
S-SET INPUT, WHEN "0", FF IS SET REGARDLESS OF INPUTS AND GATE STATES

R-RESET (CLEAR) INPUT, WHEN "0", FF IS CLEARED REGARDLESS OF INPUTS AND GATE STATES

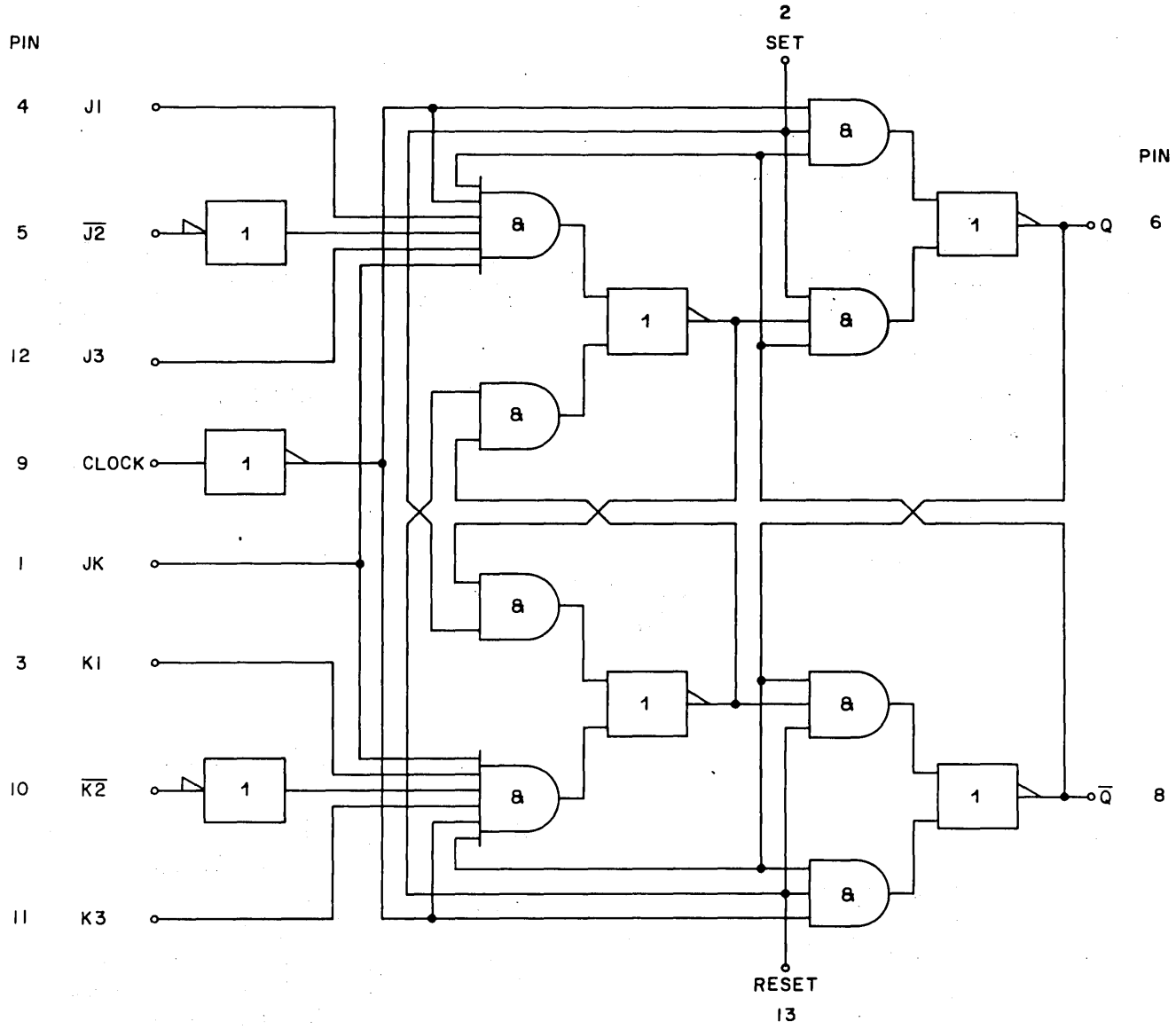
LOGIC SYMBOL

INPUTS		OUTPUTS BEFORE TOGGLE		OUTPUTS AFTER TOGGLE	
GJ	GK	SET	RESET	SET	RESET
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

TRUTH TABLE



TIMING SEQUENCE



FUNCTION DIAGRAM

Description

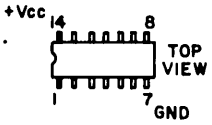
Circuit 145 is a dual expandable AND-OR-INVERT gate. Section B of this circuit is expandable. If not expanded pins 11 and 12 are open.

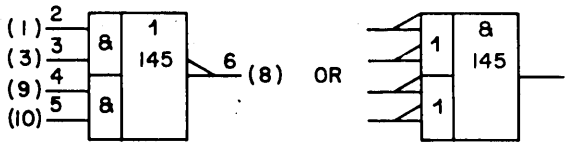
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 145 manufactured by Fairchild Semiconductors (P/N 9005).
3. Type 145H manufactured by Texas Instruments (P/N 74H50).
4. Propagation delay time:

Type	Delay Time (NSec)
145	18
145H	10

5. Package pin configuration.

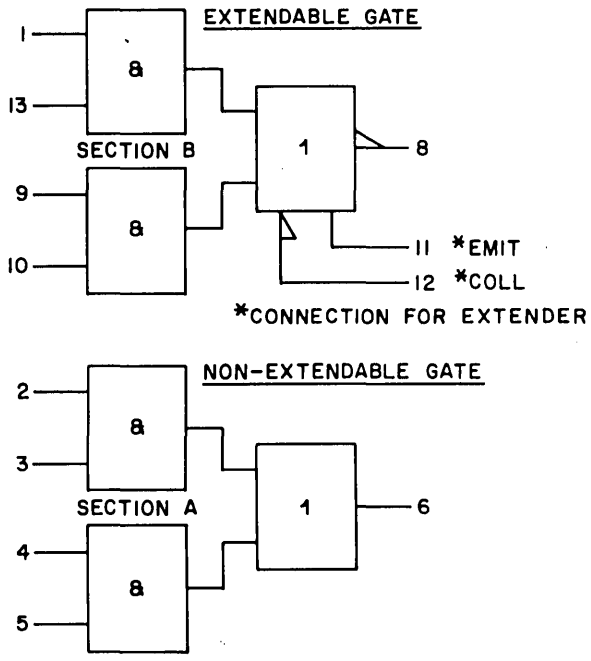




LOGIC SYMBOL

A	B	C	D	E
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	1
1	0	0	1	1
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

TRUTH TABLE



PIN ASSIGNMENTS

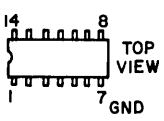
Element 145 Sheet 1 of 1

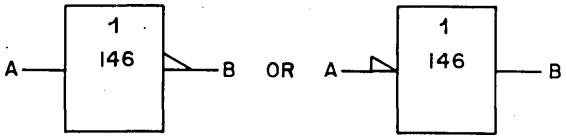
Description

The 146 circuit is a hex inverter NAND gate.

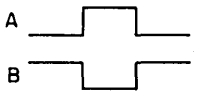
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 146 manufactured by Fairchild Semiconductors (P/N 9016).
4. Propagation delay time is 10 nsec.
5. Package pin configuration.

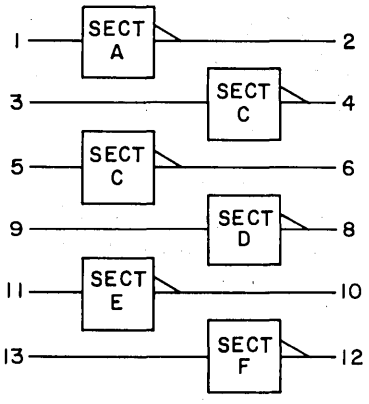




LOGIC SYMBOL



TIMING SEQUENCE



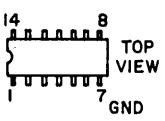
PIN ASSIGNMENTS

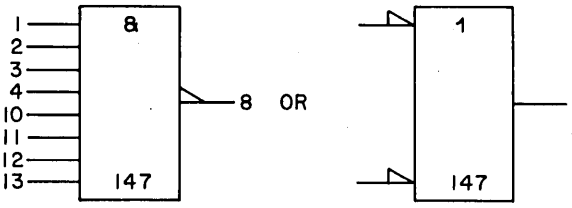
Description

The 147 circuit is a eight input-one output active low level AND/NAND gate.

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 147 manufactured by Fairchild Semiconductors (P/N 9007).
3. Propagation delay time is 18 nsec.
4. Package pin configuration.



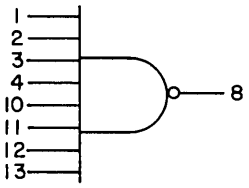


LOGIC SYMBOL

	INPUTS								OUTPUT
8	1	2	3	4	10	11	12	13	8
	H	H	H	H	H	H	H	H	L
	ANY INPUT LOW								H

	INPUTS								OUTPUT
1	1	2	3	4	10	11	12	13	8
	L	L	L	L	L	L	L	L	H
	ANY INPUT HIGH								L

TRUTH TABLE



FUNCTION DIAGRAM

148

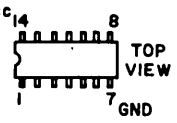
Information not available at time of printing.
It will be supplied at a later revision.

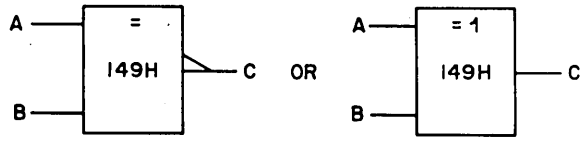
Description

The 149H circuit is a Quad 2-input Exclusive OR gate that performs the function: $Y = A\overline{B} + \overline{A}B$. When the input states are complementary, the output goes to the high level.

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 149H manufactured by Motorola Semiconductor Products, Inc., (P/N 3021).
4. Propagation delay time is 30 nsec.
5. Package pin configuration.

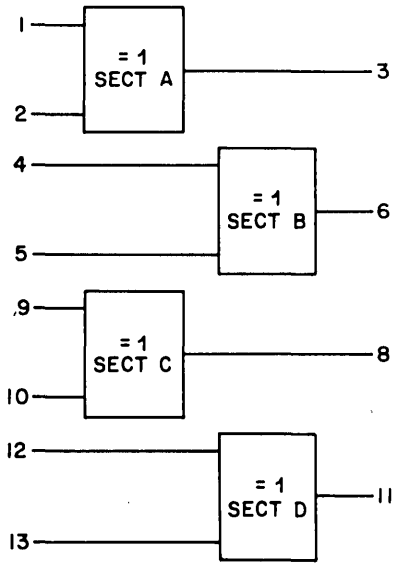




LOGIC SYMBOL

A	B	C
0	0	0
0	1	1
1	0	1
1	1	0

TRUTH TABLE



PIN ASSIGNMENTS

Element 149 Sheet 1 of 1

Description

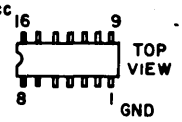
The 158 circuit is a 4-bit synchronous binary counter. This circuit can be preloaded with data at the data inputs when the load input is low. This disables the counter and enables the data inputs. Input data will be transferred to the outputs the next time the clock input has a low to high transition.

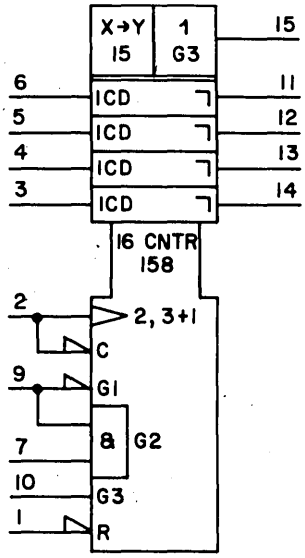
In order for the counter to count, the load, clear, enable P, and enable T inputs must be high. A low level to the clear input will clear the outputs to low level regardless of the level to any other input.

When P enable is low, the clock input is disabled so that the counter can not count when enable T is low. Also, when P enable is low, the clock input and carry output are disabled.

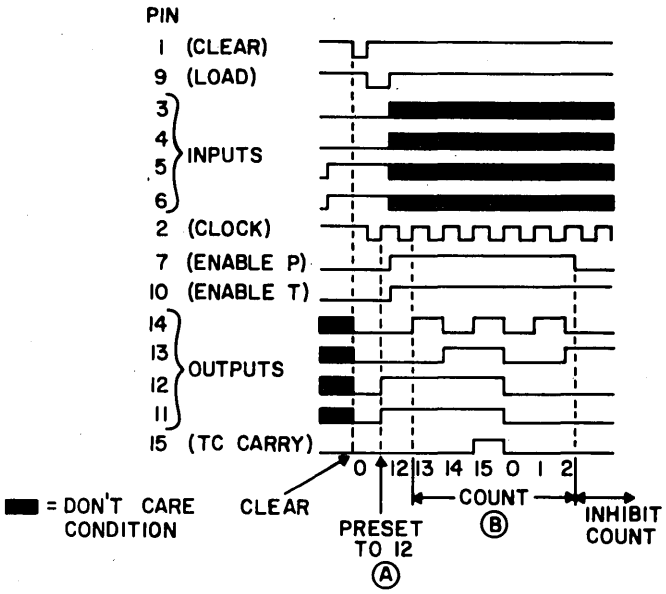
NOTES:

1. Symbol shown as it would appear on logic drawings.
2. Type 158 manufactured by Fairchild Semiconductors (P/N 9316).
3. Package pin configuration.





LOGIC SYMBOL



NOTES:

Ⓐ MODE SELECTION WITH POSITIVE-GOING CLOCK IS:

PINS 7 & 10	PIN 9	MODE
1	1	COUNT UP
0	1	NO CHANGE
1	0	PRESET
0	0	PRESET

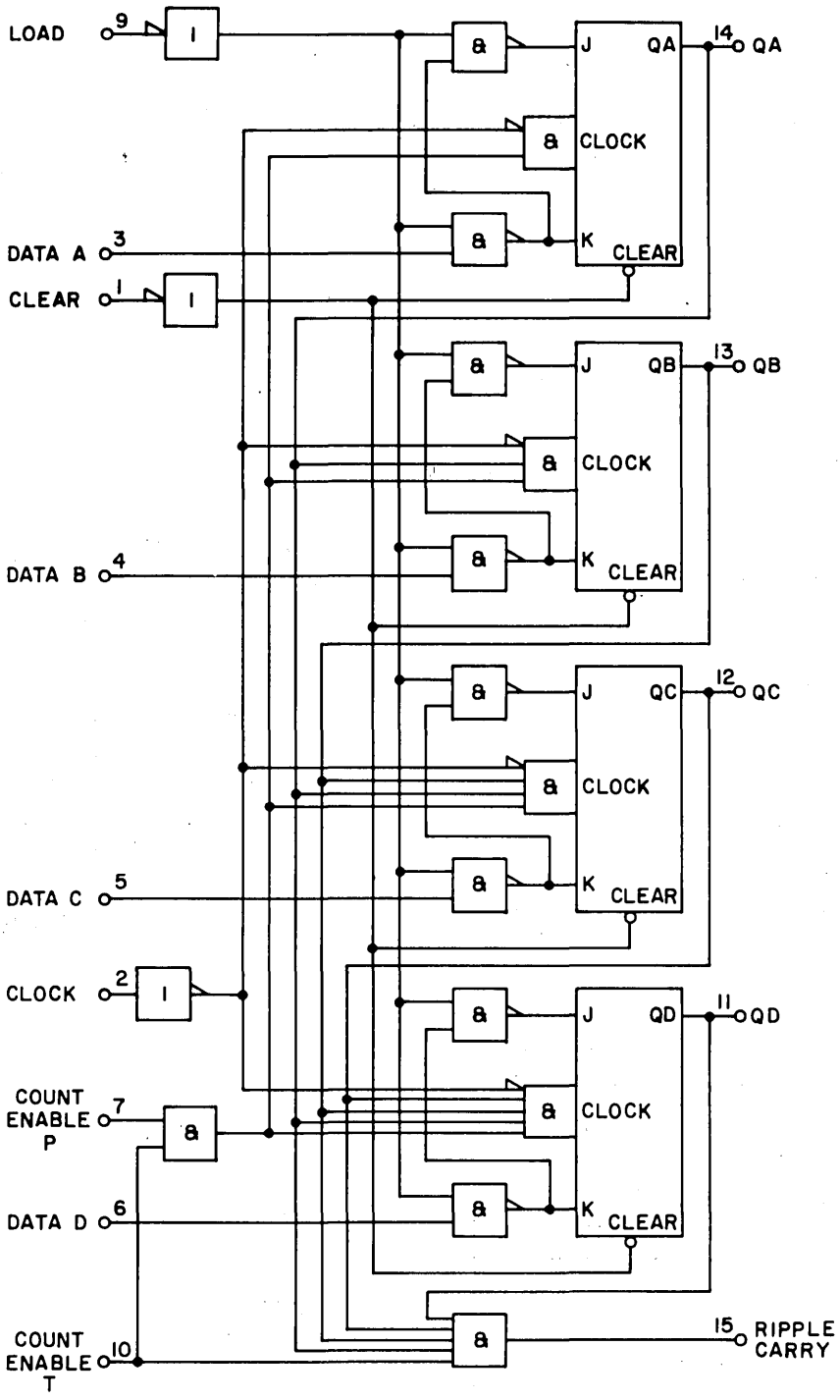
Ⓑ PIN 15 IS HIGH WHEN ALL OF THE FOLLOWING PINS ARE HIGH: 10, 11, 12, 13, AND 14.

Ⓒ ILLUSTRATED ABOVE IS THE FOLLOWING:
1. CLEAR OUTPUTS TO ZERO
2. PRESET TO BINARY 12
3. COUNT TO 13, 14, 15, 0, 1 AND 2
4. INHIBIT

Ⓓ

PIN(S)	FUNCTION
1	MASTER RESET (ACTIVE LOW) INPUT (CLEAR)
2	CLOCK ACTIVE HIGH GOING EDGE INPUT
3, 4, 5, 6	PARALLEL INPUTS
7	COUNT ENABLE PARALLEL INPUT
9	PARALLEL ENABLE (ACTIVE LOW) INPUT
10	COUNT ENABLE TRICKLE INPUT
11, 12, 13, 14	PARALLEL OUTPUTS
15	TERMINAL COUNT OUTPUT (CARRY)

TIMING SEQUENCE



FUNCTION DIAGRAM

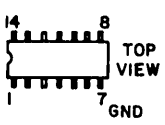
Description

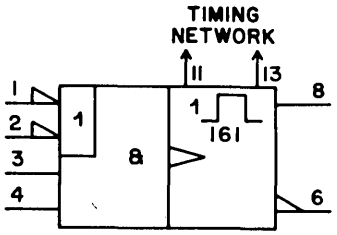
The 161 circuit is a monostable retriggerable multivibrator that provides an output pulse whose duration is a function of external timing components.

Input pins 3 and 4 trigger on the positive goine edge of the input pulse and pins 1 and 2 trigger on the negative goine input pulse. The 161 circuit will retrigger while in the pulse timing state (pin 8 high) and the end of the last pulse will be timed from the last input.

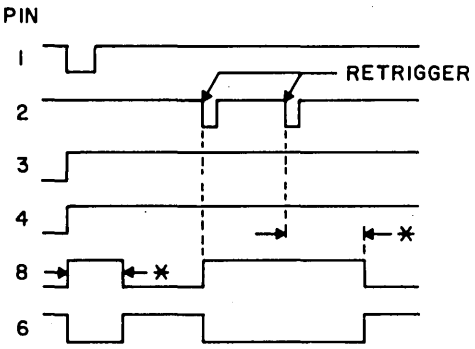
NOTES:

1. Symbol shown as it would appear on logic diagrams, except for timing network.
2. Type 161 manufactured by Fairchild Semiconductors (P/N 9601).
3. Package pin configuration.





LOGIC SYMBOL



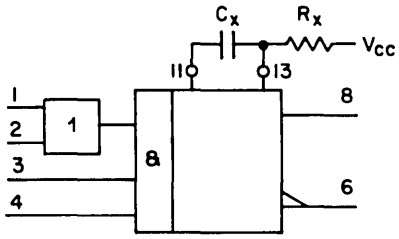
*PULSE WIDTH DETERMINED BY RC TIMING NETWORK

TIMING SEQUENCE

INPUT PINS				OPERATION	OUTPUT PINS	
1	2	3	4		8	6
H→L	H	H	H	TRIGGER	⎍	⎎
H	H→L	H	H	TRIGGER	⎍	⎎
L	X	L→H	H	TRIGGER	⎍	⎎
X	L	L→H	H	TRIGGER	⎍	⎎
L	X	H	L→H	TRIGGER	⎍	⎎
X	L	H	L→H	TRIGGER	⎍	⎎
H	H	H	H		L	H
X	X	L	X		L	H
X	X	X	L		L	H

X=DON'T CARE

TRUTH TABLE



OUTPUT PULSE WIDTH (t) IS DEFINED AS FOLLOWS:

$$t = 0.32\ R_x\ C_x \left[1 + \frac{0.7}{R_x}\right]$$

R_x IS IN KΩ, C_x IS IN pf, t IS IN NS

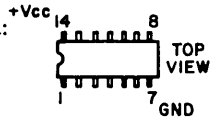
FUNCTION DIAGRAM

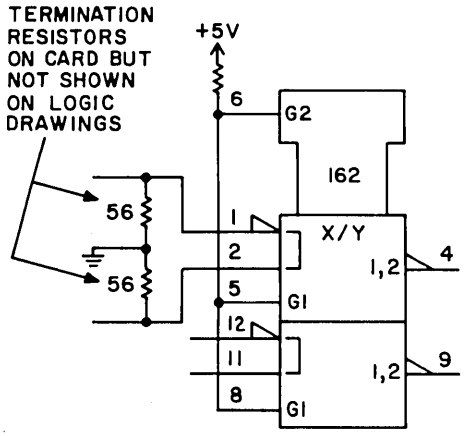
Description

The 162 circuit is a dual differential line receiver. A minimum differential voltage of 25mv is required to insure a high or low output level. Common mode voltages of ±3v or less will be rejected. The maximum allowable differential input voltage is 5 volts.

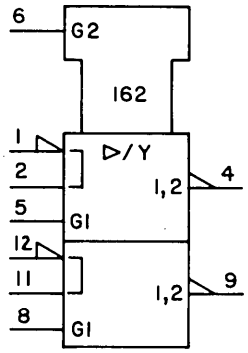
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 162 manufactured by Texas Instruments (P/N SN 75107A).
3. Type 162C manufactured by Texas Instruments (P/N SN 75108).
4. Package pin configuration:

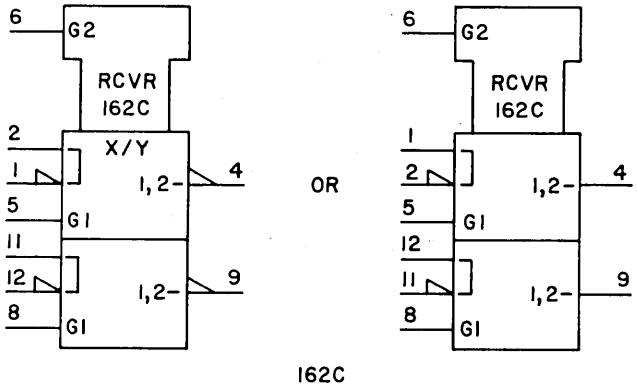




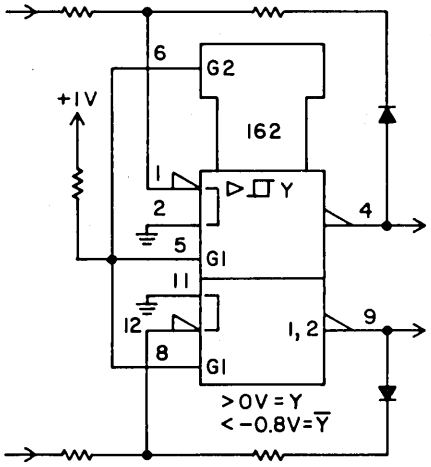
TWISTED PAIR RECEIVER APPLICATION



ANALOG TO DIGITAL CONVERTER APPLICATION



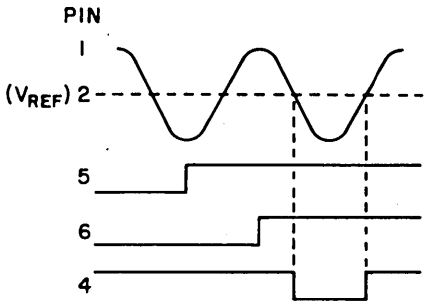
162C



162 DUAL DIFFERENTIAL RECEIVER USED AS A SCHMITT TRIGGER WITH EXTERNAL FEEDBACK NETWORKS AND FIXED BIAS ENABLING G1 AND G2 STROBE INPUTS.

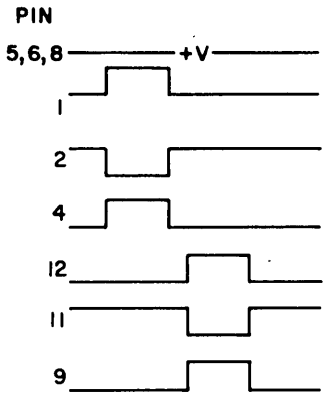
LOGIC SYMBOL

Element 162 Sheet 1 of 2

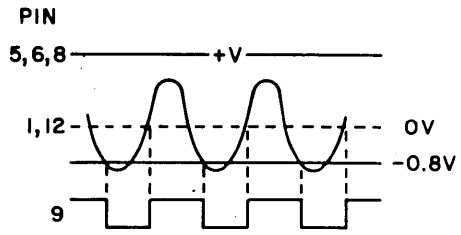


PIN 4 IS LOW ONLY IF G1 AND G2 ARE HIGH AND PIN 1 IS MORE NEGATIVE THAN PIN 2. G2 IS COMMON TO BOTH CONVERTERS.

162 DIGITAL TO ANALOG CONVERTER APPLICATION



162 TWISTED PAIR RECEIVER APPLICATION



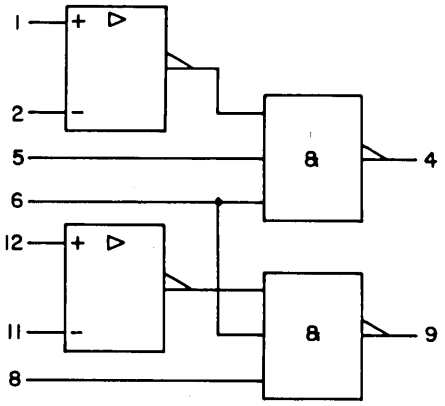
162 SCHMITT TRIGGER

TIMING SEQUENCE

DIFFERENTIAL INPUTS	STROBES		OUTPUT
	G1	G2	
$V_{ID} \geq 25MV$	L OR H	L OR H	H
$-25MV < V_{ID} < 25MV$	L OR H	L	H
	L	L OR H	H
	H	H	INDETERMINATE
$V_{ID} \leq -25MV$	L OR H	L	H
	L	L OR H	H
	H	H	L

THE DIFFERENTIAL INPUT VOLTAGE POLARITES SHOWN MEASURED AT PIN A WITH RESPECT TO PIN B. A MINUS POLARITY INDICATES THAT PIN A IS MORE NEGATIVE THAN PIN B.

TRUTH TABLE
(RCVR APPLICATION)



FUNCTION DIAGRAM

Description

The 164 circuit is a dual JK edge-triggered flip-flop. The 164 dual JK flip-flop triggers on the negative going edge of the clock. Each flip-flop is provided with a direct SET input. These direct inputs provide a means of presetting the flip-flop to initial conditions or other asychronous operations.

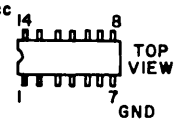
Data may be applied to or changed at the clocked inputs at any time during the clock cycle, except during the time interval between the set-up and hold-times. The inputs are inhibited when the clock is low and enabled when the clock rises. The JK inputs continuously respond to input information when the clock is high. The data state at the inputs throughout the interval between set-up and hold time is stored in the flip-flop when the clock pulse goes low. Each flip-flop may be set at any time without regard to the clock state by applying a low level to the SET input.

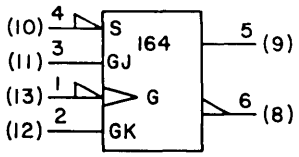
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each flip-flop.
3. Type 164H manufactured by Motorola Semiconductor Products, Inc., (P/N 3062).
4. Type 164S manufactured by Texas Instruments (P/N 74S113).
5. Propagation delay time:

Type	Delay (NSec)
164H	12
164S	7

6. Package pin configuration.

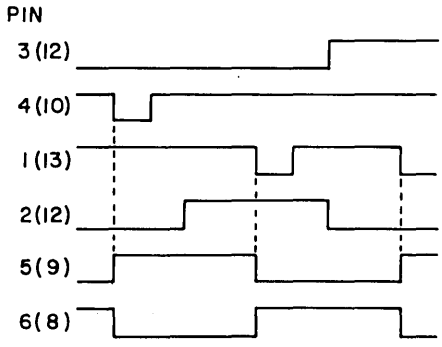




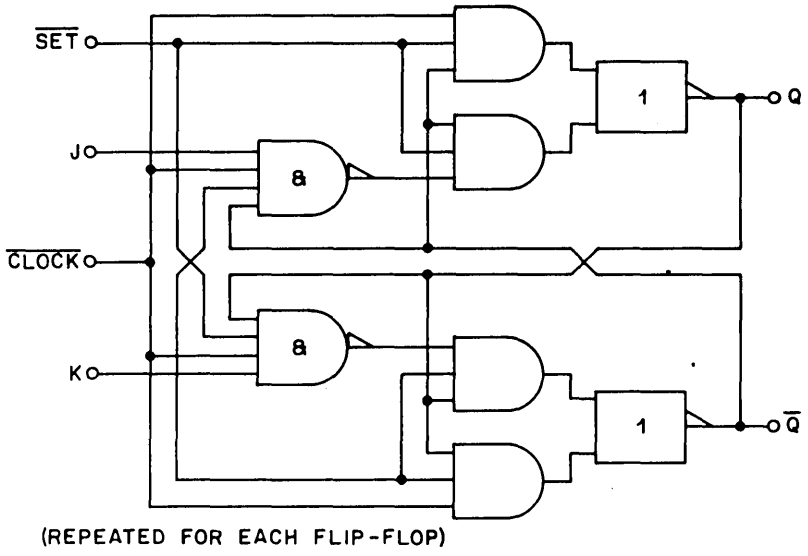
LOGIC SYMBOL

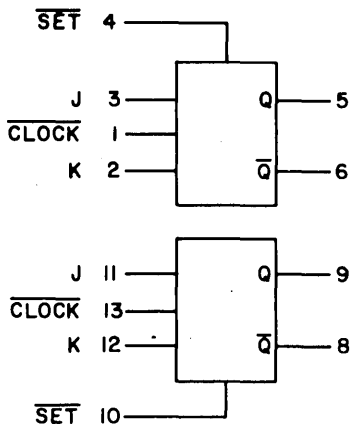
INPUT		OUTPUT BEFORE G		OUTPUT AFTER G	
J	K	SET	CLEAR	SET	CLEAR
0	0	0	1	0	1
0	0	1	0	1	0
0	1	0	1	0	1
0	1	1	0	0	1
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	1	1	0
1	1	1	0	0	1

TRUTH TABLE



TIMING SEQUENCE





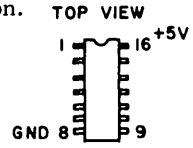
FUNCTION DIAGRAM

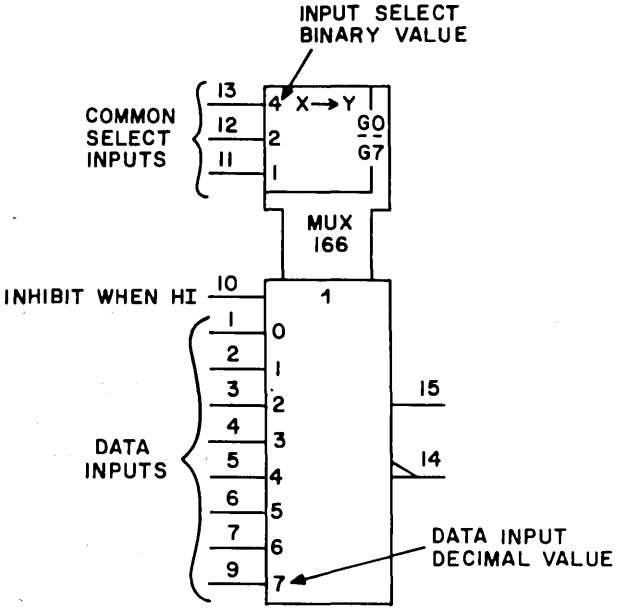
Description

The 166 circuit is an 8-bit multiplexer that can select one bit of data from up to eight sources. It has complementary outputs, an active low enable, and internal select decoding. With the enable inactive (high) the multiplexer output pin 14 is low and the complementary multiplexer output pin 15 is high regardless of all input conditions. Data is routed from a particular multiplexer input to the outputs according to the three input binary code applied to the select inputs.

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 166 manufactured by Fairchild Semiconductors (P/N 9312).
3. Package pin configuration.



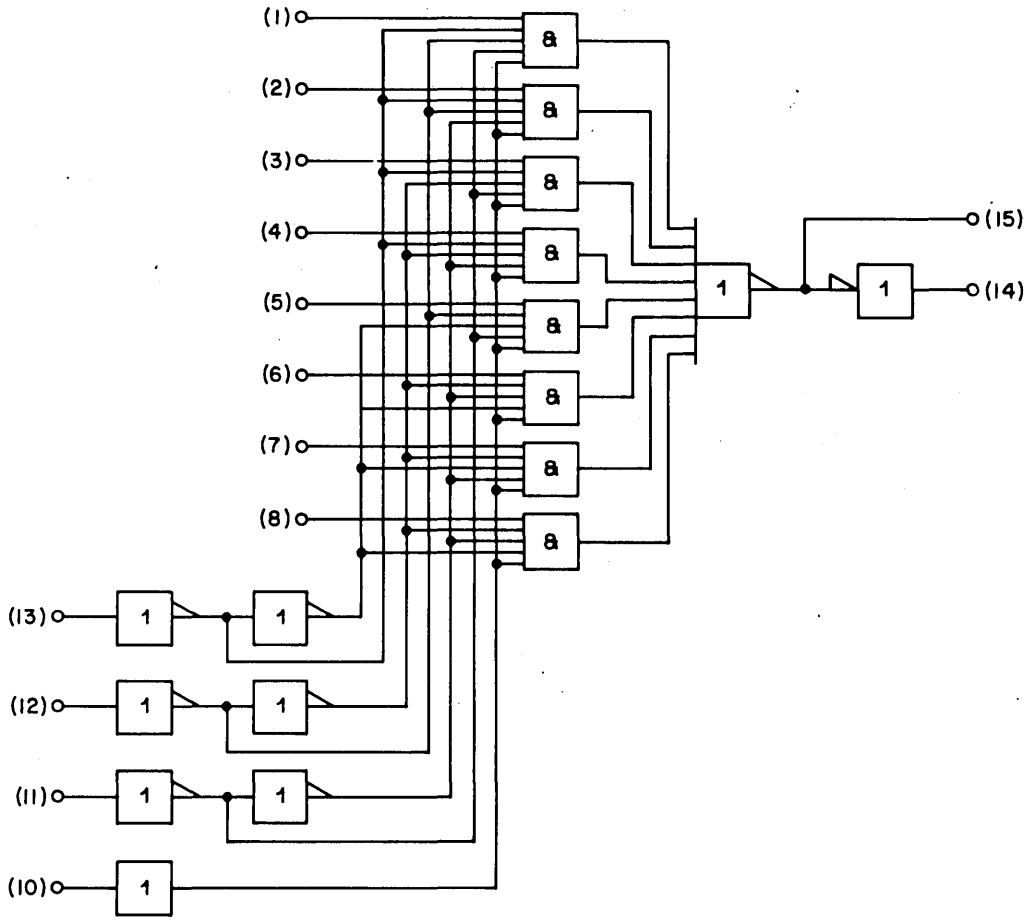


LOGIC SYMBOL

COMMON SELECT PIN			INPUT PIN GATED TO OUTPUT PIN 15* (PIN 10 LOW)
13	12	11	
0	0	0	1
0	0	1	2
0	1	0	3
0	1	1	4
1	0	0	5
1	0	1	6
1	1	0	7
1	1	1	9

* 1. OUTPUT IS HIGH IF DATA INPUT IS LOW.
2. OUTPUT IS LOW IF DATA INPUT IS LOW.
3. PIN 14 OUTPUT IS REVERSE OF PIN 15.
4. IF PIN 10 IS HIGH, PIN 15 IS LOW AND 14 IS HIGH (REGARDLESS OF SELECT/DATA INPUTS).

TRUTH TABLE



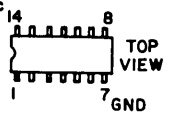
FUNCTION DIAGRAM

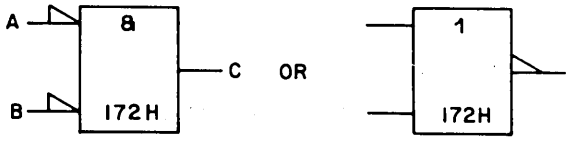
Description

The 172H circuit is a Quad 2-input NOR gate.

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 172H manufactured by Motorola Semiconductor Products, Inc., (P/N 3002).
4. Propagation delay time is 6 nsec per gate.
5. Package pin configuration.

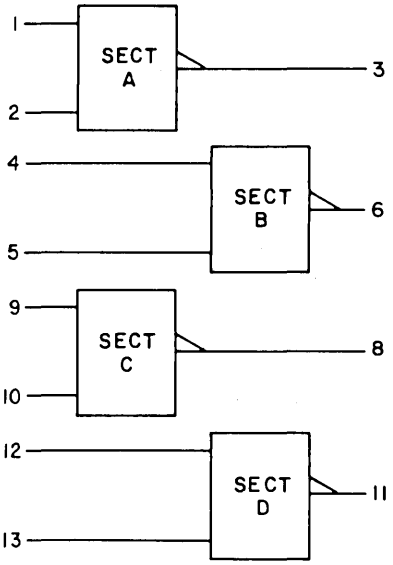




LOGIC SYMBOL

A	B	C
0	0	1
1	0	0
0	1	0
1	1	0

TRUTH TABLE



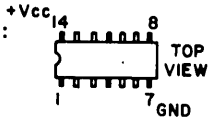
FUNCTION DIAGRAM

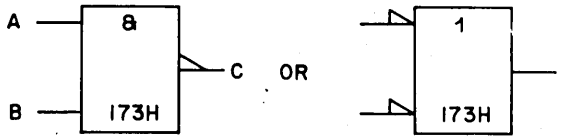
Description

The 173H circuit is an Quad 2-input NAND gate with an open collector output.

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each gate.
3. Type 173H manufactured by Motorola Semiconductor Products, Inc., (P/N 3004).
4. The output of each gate is an open collector.
5. Propagation delay time is 6 nsec per gate.
6. Package pin configuration:

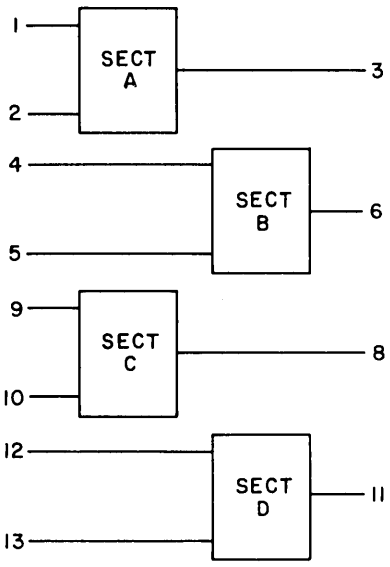




LOGIC SYMBOL

A	B	C
0	0	1
0	1	1
1	0	1
1	1	0

TRUTH TABLE



PIN ASSIGNMENTS

Element 173 Sheet 1 of 1

Description

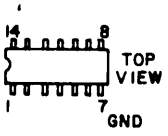
The 175H circuit is a dual flip-flop which triggers on the positive edge of the clock input pulse and performs the type D flip-flop logic function. This device consists of two completely independent Type D flip-flops, both having direct SET and RESET inputs for asychronous operations such as parallel data entry in shift register application.

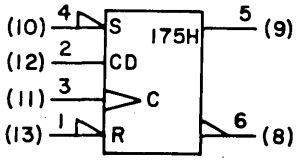
Information at input CD is transferred to output Q (pin 5/9) on the positive-going edge of the clock pulse. Clock pulse triggering occurs at a voltage level of the pulse and is not directly related to the transition time of the positive-going pulse. When the clock is at either the high or low level, the CD-input signal has no effect.

The flip-flop can also be set or cleared directly at any time regardless of the state of the clock by applying a low input to the SET or RESET inputs.

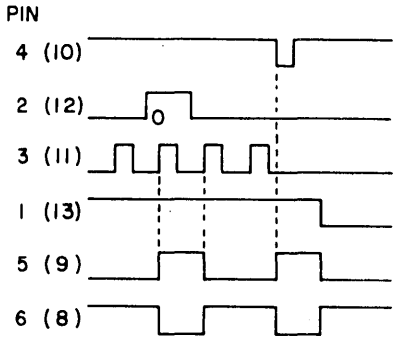
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Symbol repeated for each flip-flop.
3. Type 175H manufactured by Motorola Semiconductor Products, Inc., (P/N 3060).
4. Package pin configuration:

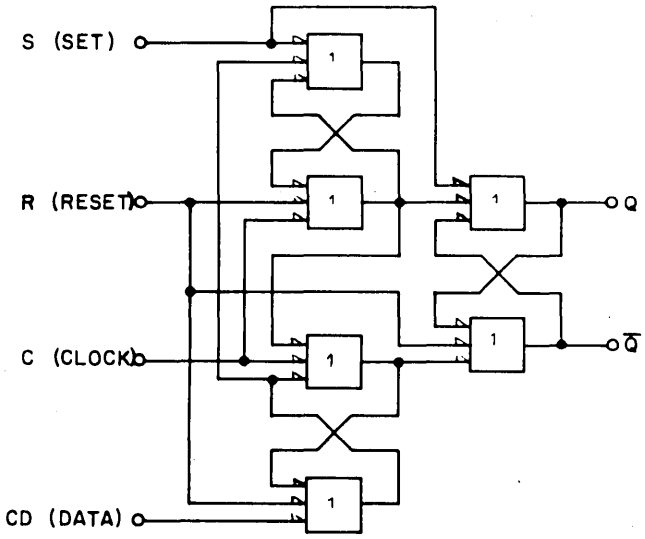




LOGIC SYMBOL



TIMING SEQUENCE



FUNCTION DIAGRAM
(EACH FLIP-FLOP)

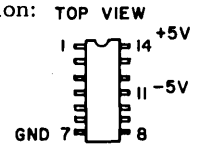
Element 175 Sheet 1 of 1

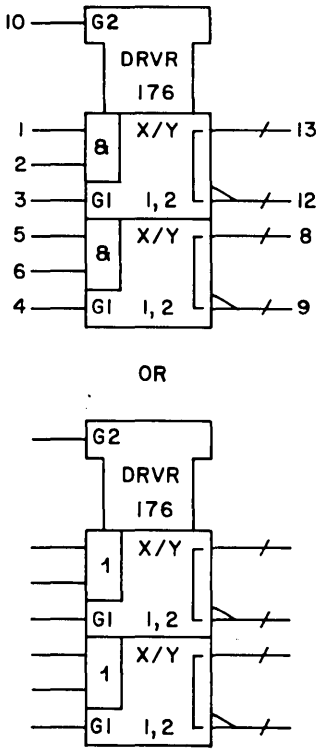
Description

The 176 circuit is a dual differential line driver. This circuit accepts a DTL or TTL logic signal and transmits it over a differential line pair. On state output current is typically 12 ma. Off state output current is 100 ma max. The output common mode voltage range is -3v to +10v with respect to the circuit ground.

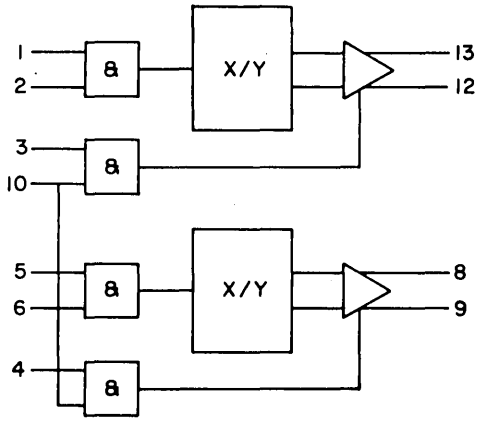
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 176 manufactured by Texas Instruments (P/N SN 75110).
3. Package pin configuration:

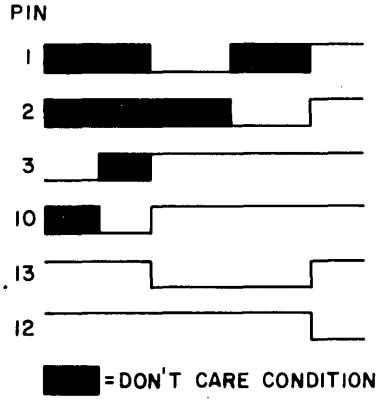




LOGIC SYMBOL



FUNCTION DIAGRAM



TIMING SEQUENCE

LOGIC INPUTS		INHIBIT INPUTS		OUTPUTS*		OUTPUT CONDITION
1, 5	2, 6	3, 4	10	9, 12	8, 13	
1 OR 0 1 OR 0	1 OR 0 1 OR 0	0 1 OR 0	1 OR 0 0	1 1	1 1	INHIBITED
0 1 OR 0 1	1 OR 0 0 1	1 1 1	1 1 1	0 0 1	1 1 0	ACTIVE DATA STATE

*LOW OUTPUT REPRESENTS THE CURRENT ON STATE.
HIGH OUTPUT REPRESENTS THE CURRENT OFF STATE.

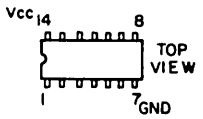
TRUTH TABLE

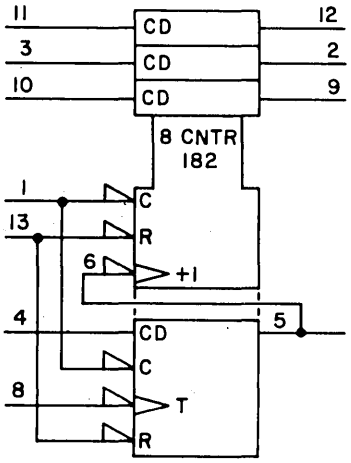
Description

Circuit type 182 is a 4 bit binary counter. During the count operation, transfer of information to the outputs occurs on the negative-going edge of the clock pulse. The direct clear (pin 13) when taken low, sets all outputs low regardless of the states of the clocks (pins 8 and 6). The 182 counter is fully programmable; that is, the outputs may be preset to any state by placing a low ("0") on the count/load input (pin 1) and entering the desired data at the inputs. The outputs will change to agree with the data inputs independent of the state of the clock inputs.

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 182 manufactured by Texas Instruments (P/N SN 74197) or Signetics Corporation (P/N 8291).
3. Package pin configuration

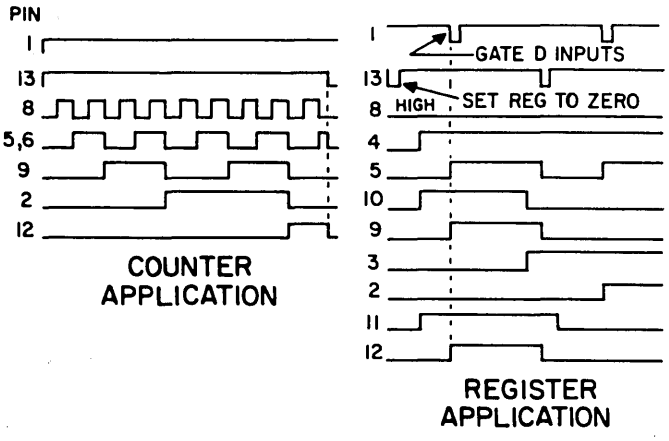




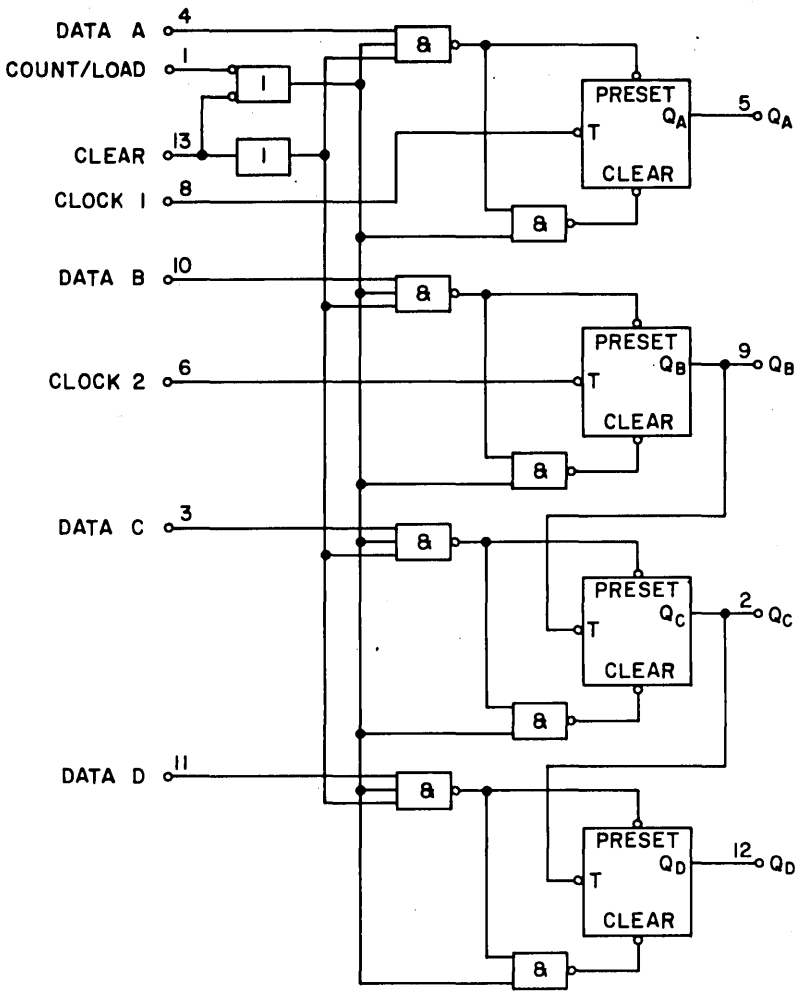
LOGIC SYMBOL

COUNT	OUTPUT			
	Q_D	Q_C	Q_B	Q_A
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1
10	1	0	1	0
11	1	0	1	1
12	1	1	0	0
13	1	1	0	1
14	1	1	1	0
15	1	1	1	1

TRUTH TABLE
(WITH PINS 5 AND 6 WIRED TOGETHER)



TIMING SEQUENCE

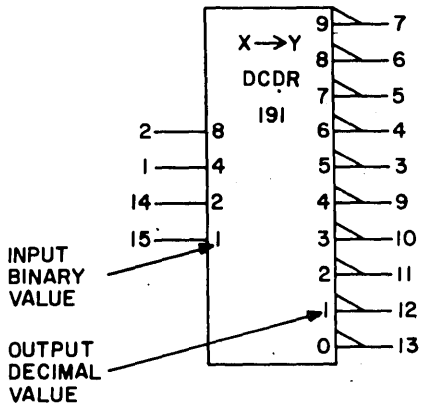


FUNCTION DIAGRAM

Description

Circuit type 191 is a BCD-to-decimal (1 of 10) decoder. Four active high BCD inputs provide one of ten mutually exclusive active low outputs. When a binary code greater than 9 is applied, all outputs are high. This facilitates BCD to decimal conversions and eight channel demultiplexing and decoding.

The 191 circuit can serve as a one of eight decoder with the D input acting as the active low enable. Eight channel demultiplexing results when data is applied to the D input and the desired output is addressed by inputs A, B, and C.



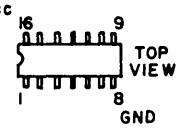
LOGIC SYMBOL

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 191 manufactured by Fairchild Semiconductors (P/N 9301).
3.

Pin	Function
1, 2, 14, 15	Address inputs
3-7, 9-13	Outputs (active low)

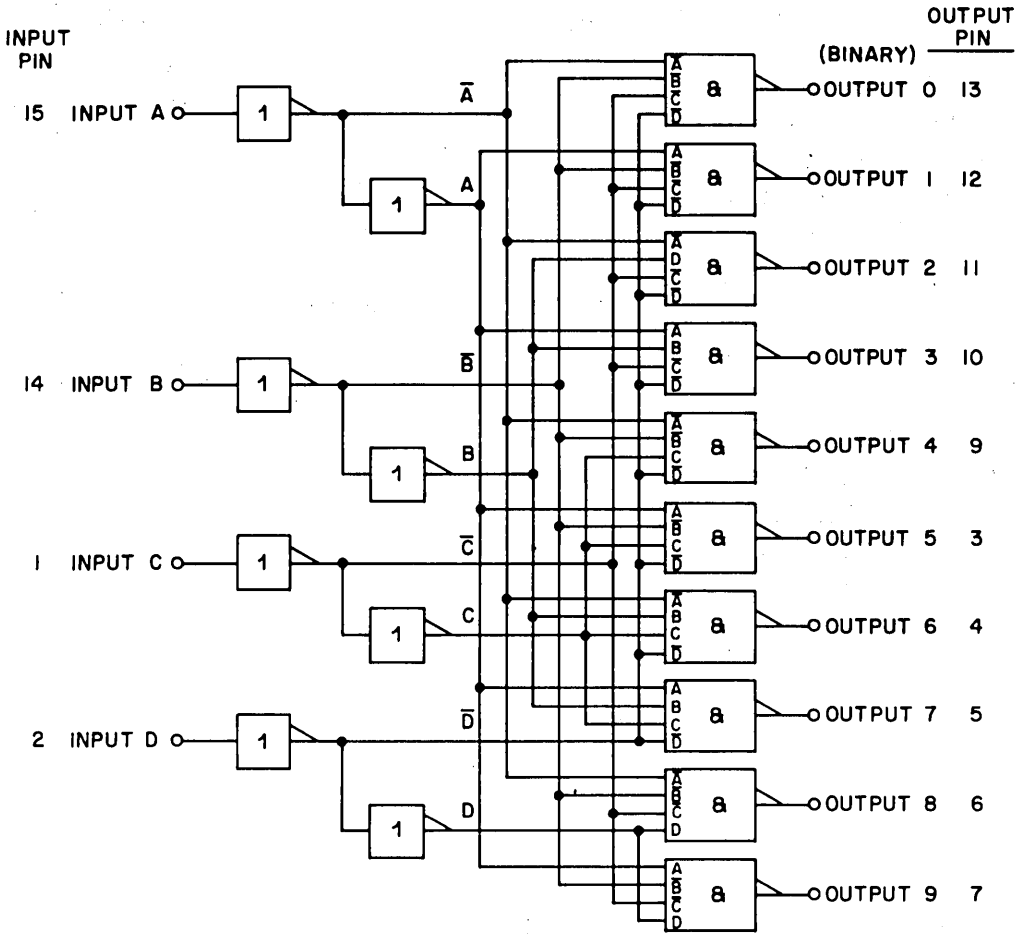
4. Package pin configuration:



INPUT PIN				LO ("0") OUTPUT PIN (OTHER OUTPUTS = "1"
2	1	14	15	
0	0	0	0	13
0	0	0	1	12
0	0	1	0	11
0	0	1	1	10
0	1	0	0	9
0	1	0	1	3
0	1	1	0	4
0	1	1	1	5
1	0	0	0	6
1	0	0	1	7
1	0	1	0	*
1	0	1	1	*
1	1	0	0	*
1	1	0	1	*
1	1	1	0	*
1	1	1	1	X

* = ALL OUTPUT PINS HIGH

TRUTH TABLE



FUNCTION DIAGRAM

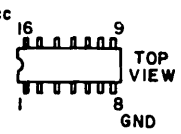
Description

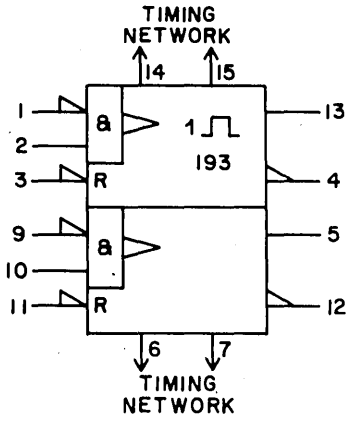
The 193 circuit is a retriggerable monostable multivibrator. Triggering the input before the output pulse is terminated extends the output pulse duration. The overriding clear input (pin 3/11) permits any output pulse to be terminated at a predetermined time independently of the timing network.

Successive triggering inputs having a period shorter than the delay time produce a constant high output.

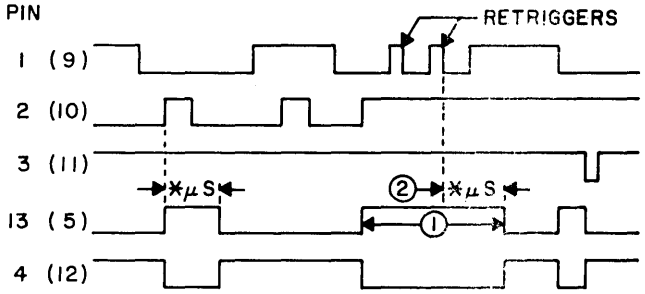
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 193 manufactured by Texas Instruments (P/N 74123).
3. Package pin configuration:



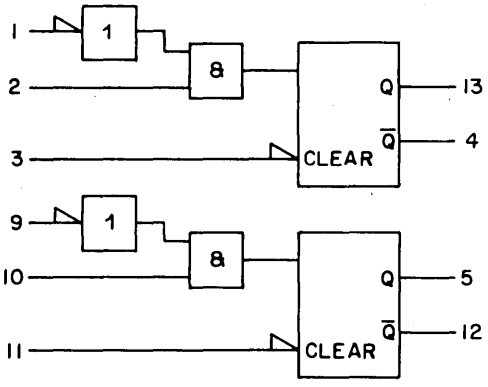


LOGIC SYMBOL



* PULSE DURATION IS A FUNCTION OF THE RC TIMING NETWORK.
① OUTPUT HELD HIGH DURING RETRIGGER PULSE.
② OUTPUT TIMES OUT FROM EDGE OF LAST TRIGGER PULSE.

TIMING SEQUENCE



FUNCTION DIAGRAM

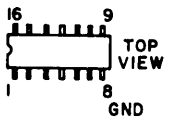
Description

The 195 circuit is a dual monostable retriggerable multivibrator that provides an output pulse whose duration is a function of external timing components.

Input pins 4 and 12 trigger on the positive going edge of the input pulse and pins 5 and 11 trigger on the negative going input pulse. The 195 circuit will retrigger while in the pulse timing state (pin 8 high) and the end of the last pulse will be timed from the last input. A low level to the reset input (pin 3/13) resets pin 6/10 to low level and inhibits data inputs.

NOTES:

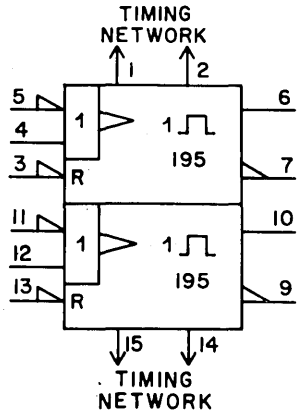
1. Symbol shown as it would appear on logic diagrams, except for timing network.
2. Type 195 manufactured by Fairchild Semiconductors (P/N 9602).
3. Package pin configuration.



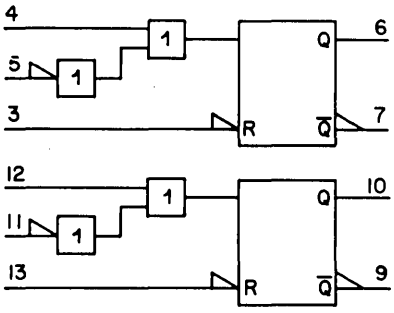
4. H = high level (steady state), L = low level (steady state), ↑ = transition from low to high level, ↓ = transition from high to low level, ⎍ = one high-level pulse, ⎎ = one low level pulse, X = irrelevant (any input, including transitions).
5. Output pulse width (t) is defined as follows:

$$t = 0.32\ R_X\ C_X \left[1 + \frac{0.7}{R_X}\right]$$

R_X is in KΩ, C_X is in pf, t is in ns



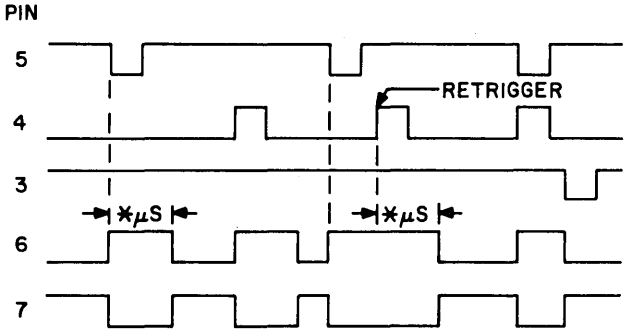
LOGIC SYMBOL



FUNCTION DIAGRAM

INPUTS		OUTPUTS	
A	B	Q	$\overline{Q}$
H	X	L	H
X	L	L	H
L	↑	⎍	⎎
↓	H	⎍	⎎

TRUTH TABLE
(SEE NOTE 4)



* PULSE DURATION IS A FUNCTION OF THE RC TIMING NETWORK.

TIMING SEQUENCE

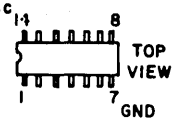
Element 195 Sheet 1 of 1

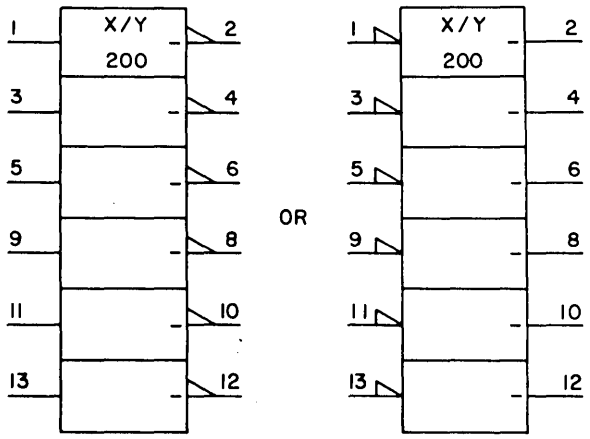
Description

The 200 circuit is a hex inverter buffer/driver with an open collector output.

NOTES:

1. Symbol shown as it would appear on logic diagrams (symbol sections may appear separately).
2. Type 200 manufactured by Texas Instruments (P/N 7406).
3. Propagation delay time 10-15 nsec typical.
4. Package pin configuration.





LOGIC SYMBOL

202S

Information not available at time of printing.
It will be supplied at a later revision.

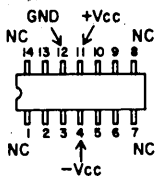
Information not available at time of printing.
It will be supplied at a later revision.

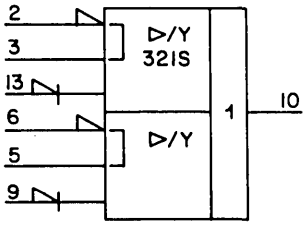
Description

The 321S is a dual differential comparator. Output, pin 10, is high when either pin 2 is at a lower potential than pin 3 and pin 13 is high, or pin 6 is at a lower potential than pin 5 and pin 9 is high. A low level to pin 9 or 13 will inhibit operation of that section which it controls.

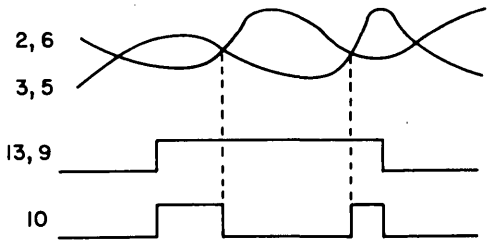
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 321S manufactured by Transitron Electronics (P/N TSC 5711).
3. Package pin configuration.





LOGIC SYMBOL



FUNCTION SEQUENCE

339

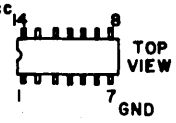
Information not available at time of printing.
It will be supplied at a later revision.

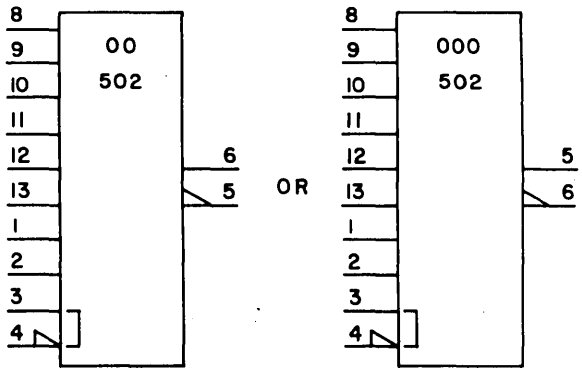
Description

The 502 circuit is a 8-bit parity generator/checker with complementry outputs and control inputs to facilitate operation in either odd-or even-parity applications.

NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 502 manufactured by Texas Instruments (P/N SN74180).
3. Package pin configuration.



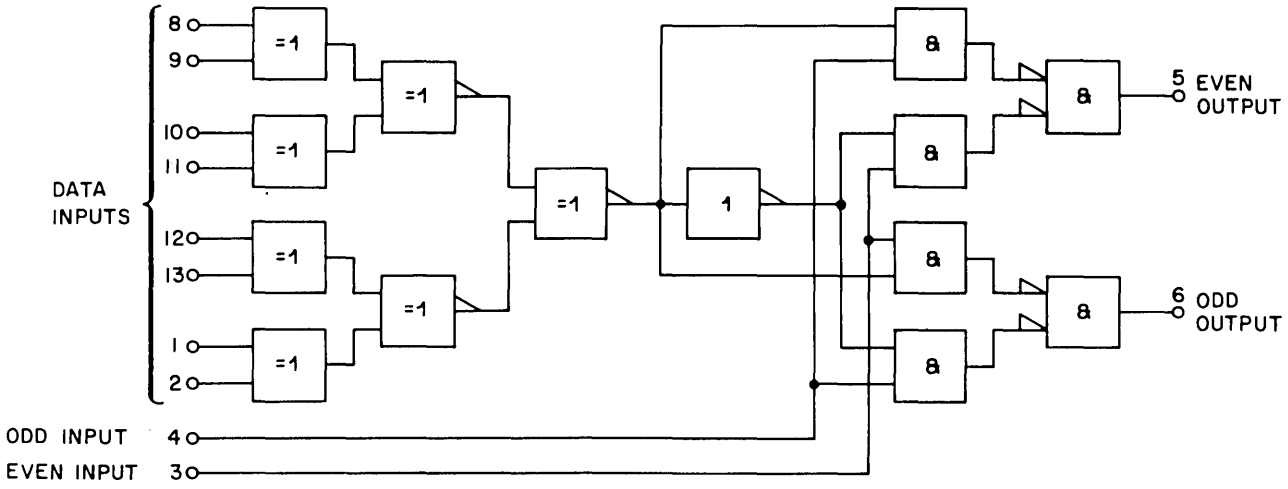


LOGIC SYMBOL

INPUTS			OUTPUTS	
Σ OF 1's AT PINS 1, 2, 8 THRU 13	PIN 3	PIN 4	PIN 5	PIN 6
EVEN	1	0	1	0
ODD	1	0	0	1
EVEN	0	1	0	1
ODD	0	1	1	0
X	1	1	0	0
X	0	0	1	1

X = IRRELEVANT

TRUTH TABLE



FUNCTION DIAGRAM

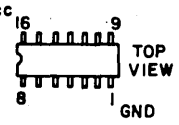
Element 502 Sheet 1 of 1

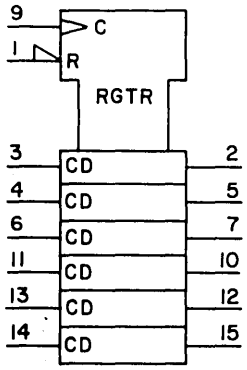
Description

The 519 circuit is a register made up of hex D-type flip-flops with clear input.

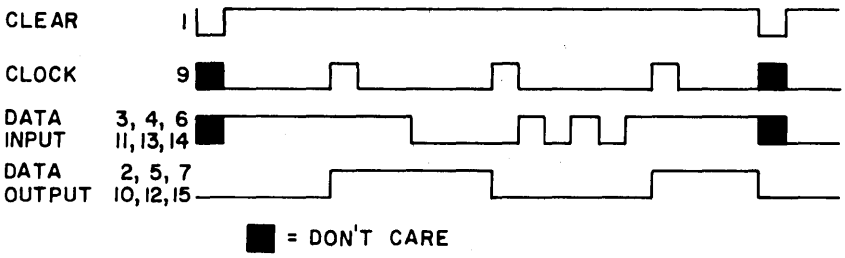
NOTES:

1. Symbol shown as it would appear on logic diagrams.
2. Type 519 manufactured by Texas Instruments (P/N SN 74174).
3. Package pin configuration.

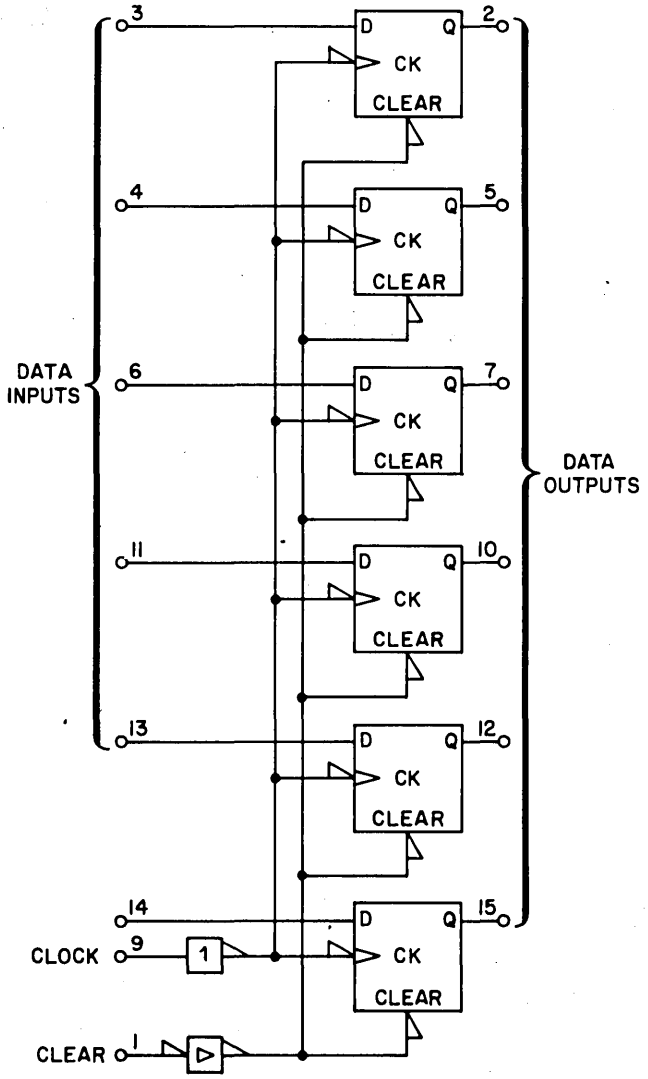




LOGIC SYMBOL



FUNCTION SEQUENCE



FUNCTION DIAGRAM

916

Information not available at time of printing.
It will be supplied at a later revision.

926

Information not available at time of printing.
It will be supplied at a later revision.

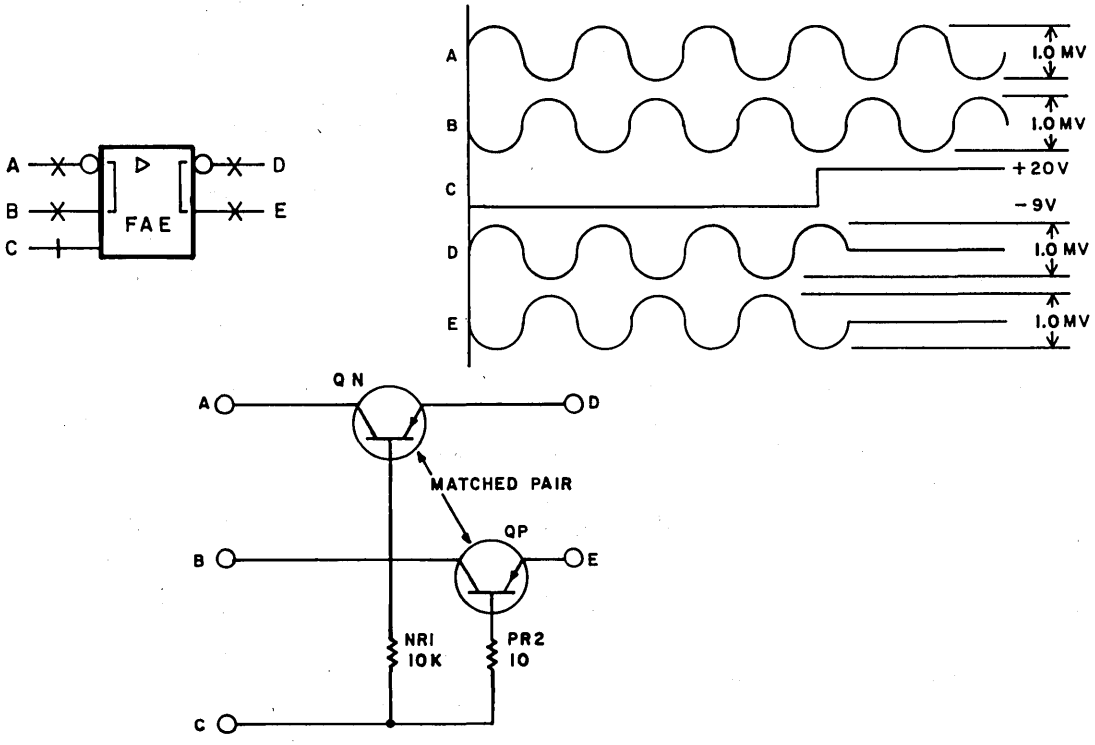
Information not available at time of printing.
It will be supplied at a later revision.

SECTION 6

DISCRETE COMPONENT CIRCUITS

GATED AMPLIFIER - FAE

The FAE circuit consists of two matched transistors acting as low level analog gates. Inputs A and B receive the output of differential windings of a read head. Output points D and E drive the input of a low level amplifier such as an FAF. The outputs are gated by input C. When point C is at -9 volts, QN and QP turn on enabling data to flow from points A and B to C and D respectively. At +20 volts on point C, QN and QP turn off, inhibiting the output.



NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

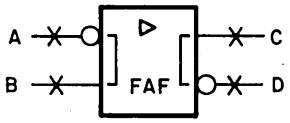
7J10

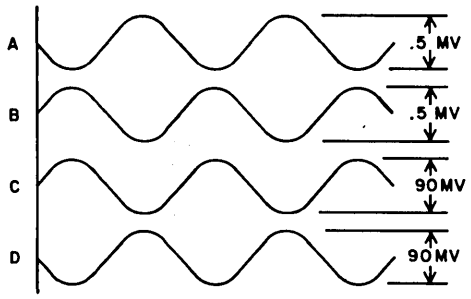
AMPLIFIER - FAF

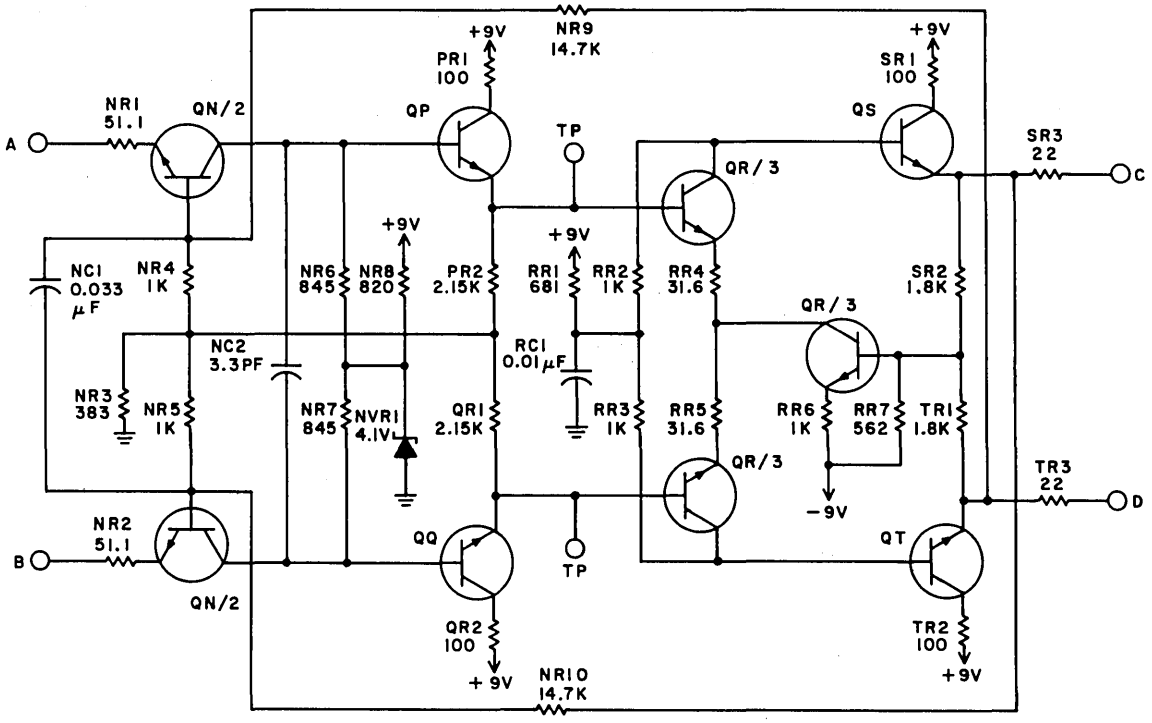
The FAF circuit is a low level amplifier that amplifies analog read signals. Points A and B are typically connected to Gated Amplifiers which provide biasing for the common base input stage.

The amplifier consists of two stages, common base first stage (QN matched pair) and common emitter second stage (QR matched pair) with emitter follower outputs (QS and QT) for low output impedance. The gain of the first stage is dependent upon the signal source resistance and is approximately 9 with 9750 type heads as a signal source. The gain of the second stage is approximately 20, therefore, the overall amplifier gain is approximately 180.

DC feedback is provided by NR9, NR10,PR2 and QR1 to the base circuitry of the QN matched pair. This feedback helps to stabilize the DC operating points in the circuit. Capacitor NC1 provides a lower impedance path between bases of the input transistors which presents a low amplifier input impedance for AC signals over the passband of the amplifier.







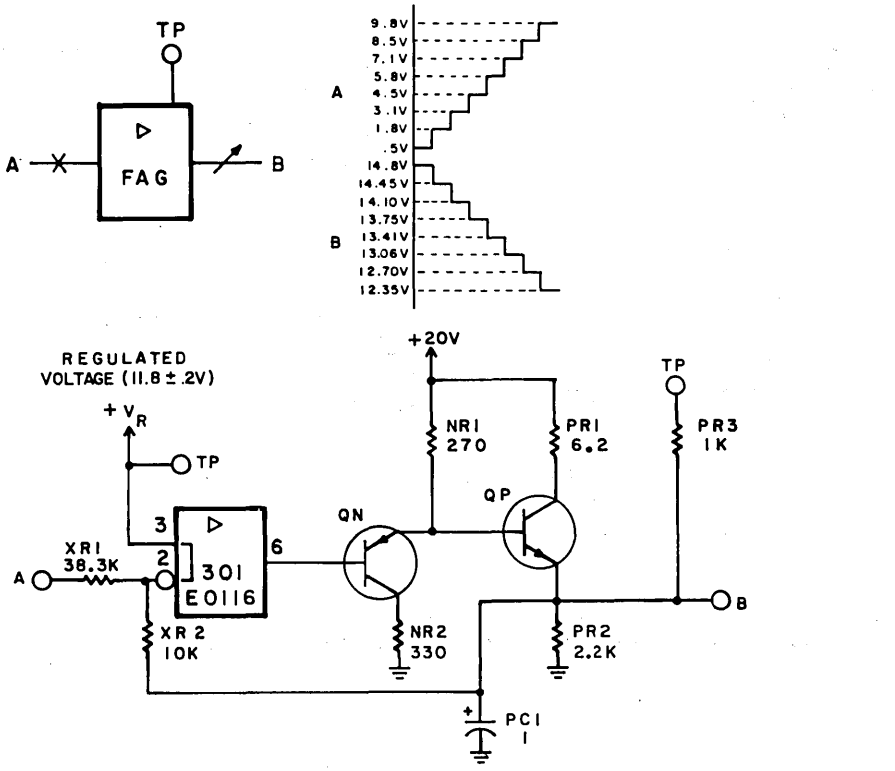
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7JII

CONTROLLED VOLTAGE SOURCE - FAG

The FAG circuit is a controlled voltage source providing a controlled voltage to Write Driver - JAG.

The circuit consists of an operational amplifier and a two transistor buffer extends the output current capability. The transistor buffer is included in the negative feedback circuit to reduce the output voltage change due to temperature variation.

The output at B (V_B) is related to the two inputs V_R and A(V_A) by the following expression: $V_B = V_R \left(1 + \frac{XR2}{XR1}\right) - \frac{XR2}{XR1} V_A$

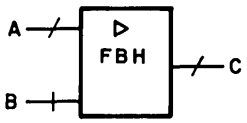


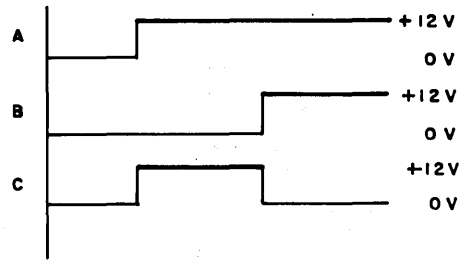
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J12B

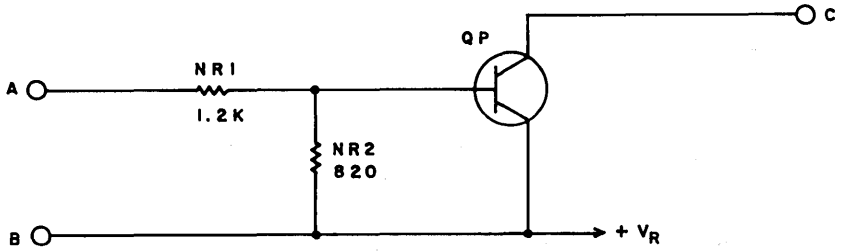
VOLTAGE SWITCH - FBH

The FBH is a voltage switch which transfers a voltage at input B to output C when QP is turned on by the proper voltage condition at input A.

In a typical circuit the voltage at input B is +12 volts. With 0 volts applied to input A, transistor QP turns on and output C goes to +12 volts. When input B is open (as when connected to an open collector IC that is turned off) QP will turn off and output C will be disconnected from input B and return to any quiescent potential in the circuit it is connected to.







NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J114

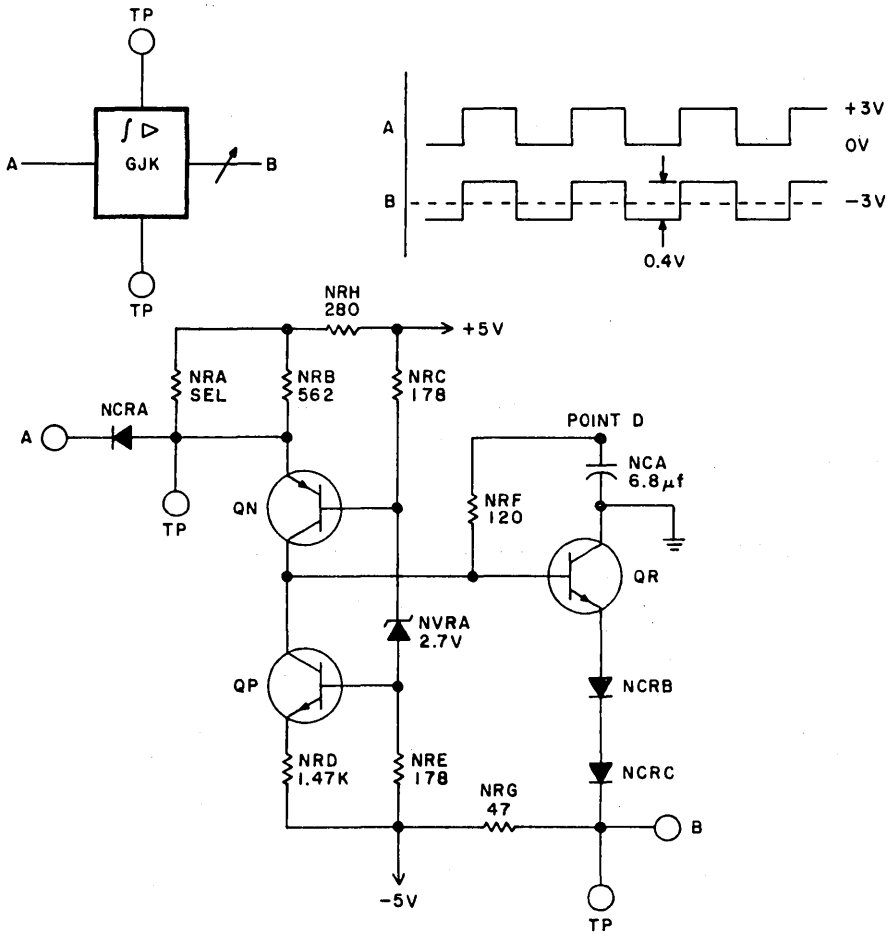
LOW PASS FILTER AND AMPLIFIER - GJK

The GJK circuit consists of a bidirectional current pump, a filter, and a level shifter. The circuit converts TTL input signals from a comparator circuit and integrates these signals to produce a dc voltage level at output B. Because of the phase locked oscillator closed loop, the current pump drives the dc level at point D to reach a steady state when the signal at input A is a square waveform. Frequency synchronism has been achieved at this point. A change in data frequency (duty cycle) causes a change in average ac voltage across NRF.

NRC, NVRA, and NRE form a reference voltage divider for the current pump. NRD and QP is the negative-going current sink. This sinks a current of approximately 2 ma continually. NCRA, NRA, NRB, and QN form a switchable current source of approximately 15 ma. When a square wave TTL logic level is applied to input A, NCA alternately is charged and discharged by 5 ma. The charge/discharge times under normal operating conditions are long compared to the input pulse times, therefore, the voltage across NCA has very little ac component in it.

Resistor NRF generates an ac component to ride on the dc voltage existing across NCA. This ac component is controlled by the value of NRF and the currents from the bidirectional pump. The net result at the base of QR is a dc voltage which corresponds to a particular input data frequency with a square waveform superimposed on it for phase synchronism purposes.

QR, NCRB, NCRC, and NRG form a buffer and level shifting circuit. They shift the waveform at the base of QR negatively to a level appropriate for voltage control oscillator frequency.



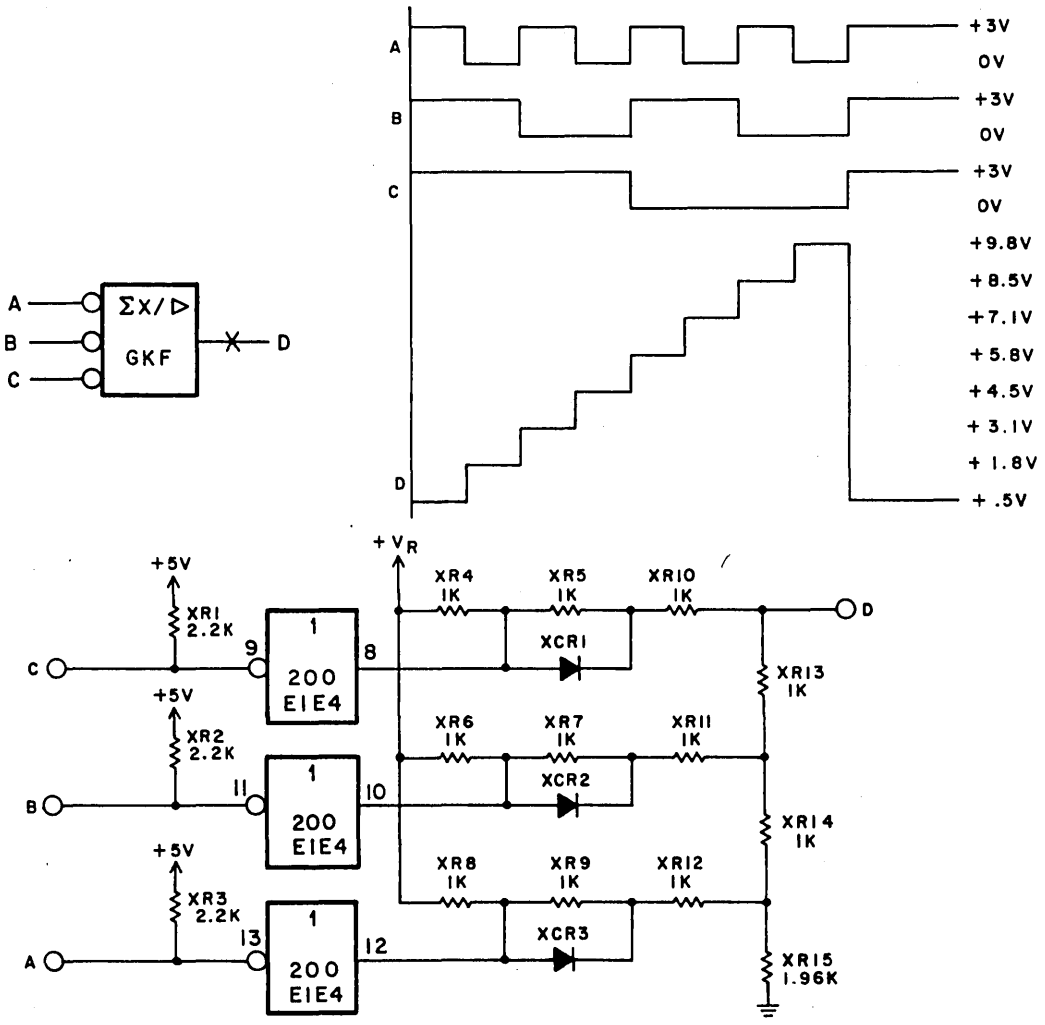
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J170

DIGITAL TO ANALOG CONVERTER - GKF

The GKF circuit converts three digital input signals to an analog output whose level depends upon the logical combination at the inputs.

The element 200 is an open collector IC. When pin 9 of element 200 is +3 volts or a "1", its output (pin 8) is 0 volts. When pin 9 is 0 volts or a "0", its output (pin 8) is open and the resistor divider (XR4, XR10, XR13, etc.) to V_r determine the voltage at an identical manner but have less influence on the voltage at point D because of their entry connection in the resistor network.

When V_r is +12 volts the output at D corresponding with the various combinations of logic input is as shown in the waveform diagram.



NOTE:
VOLTAGE AND COMPONENENT VALUES ARE FOR REFERENCE ONLY. 7J14

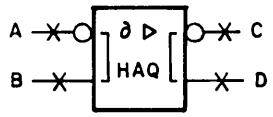
DIFFERENTIATOR/AMPLIFIER - HAQ

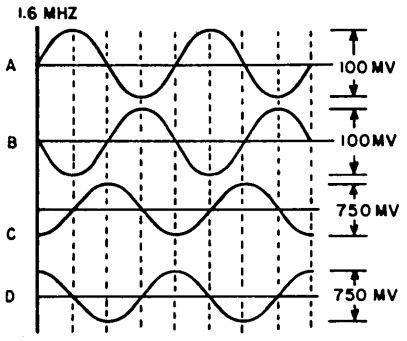
The HAQ circuit consists of a passive RC network (used as a differentiator and a differential amplifier) to boost the attenuated signal level.

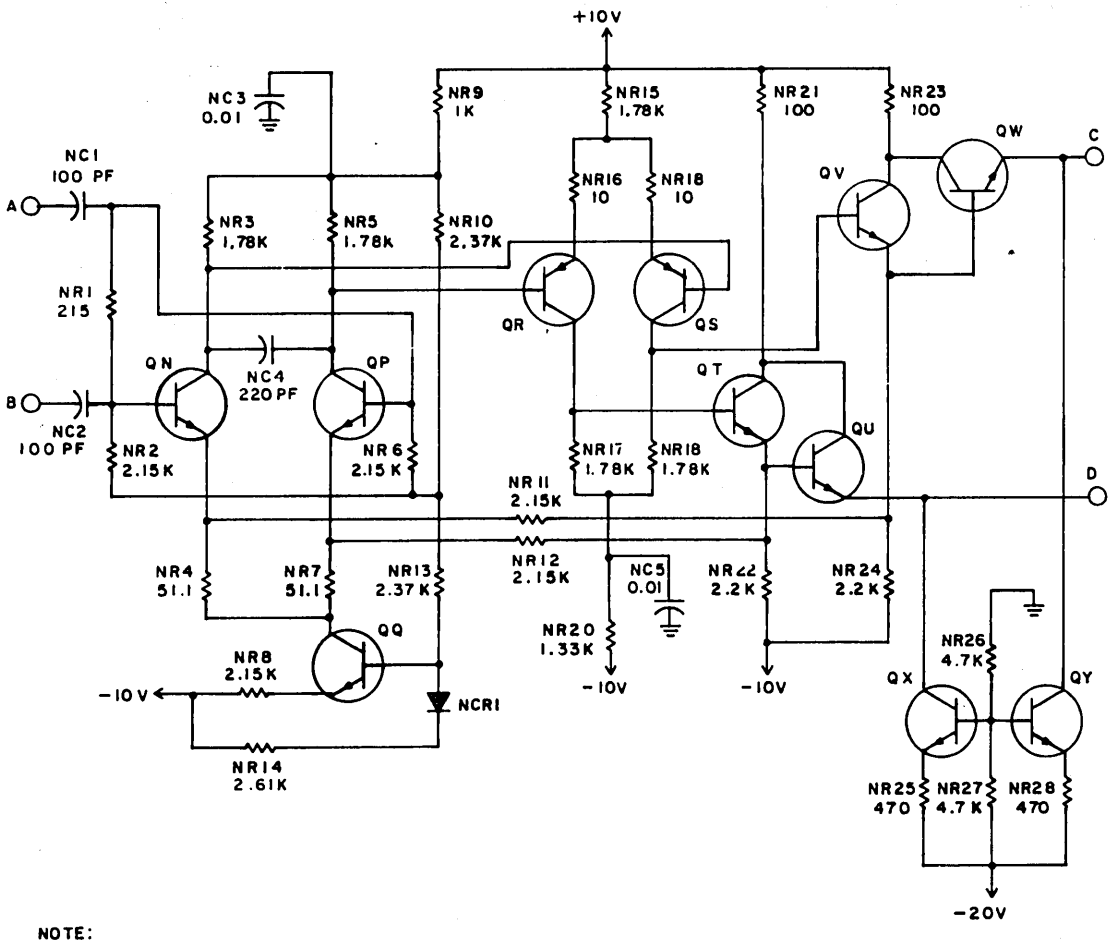
The HAQ, inputs A and B, are connected to outputs D and E of circuit HAP, which supplies an amplified read head signal. NC1, NR1, and NR2 make up the differentiator which has a break frequency at 15 MHz.

The two stage differential amplifier consists of first stage QN and QP with current sink QQ direct coupled to second stage QR and QS. QT, QU and QV, QW form darlington emitter followers for low output impedance capable of driving coax lines terminated by 100 ohm resistors. QX and QY are constant current sources.

NR11 and NR12 provide AC/DC feedback from the output to input emitters of the first stage. Closed loop voltage gain is proportional to the ratio, NR11 to NR4 (and NR12 to NR7). Capacitor NC4 provides roll-off at the upper cutoff frequency.







NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J20A

RECTIFIER - HBA

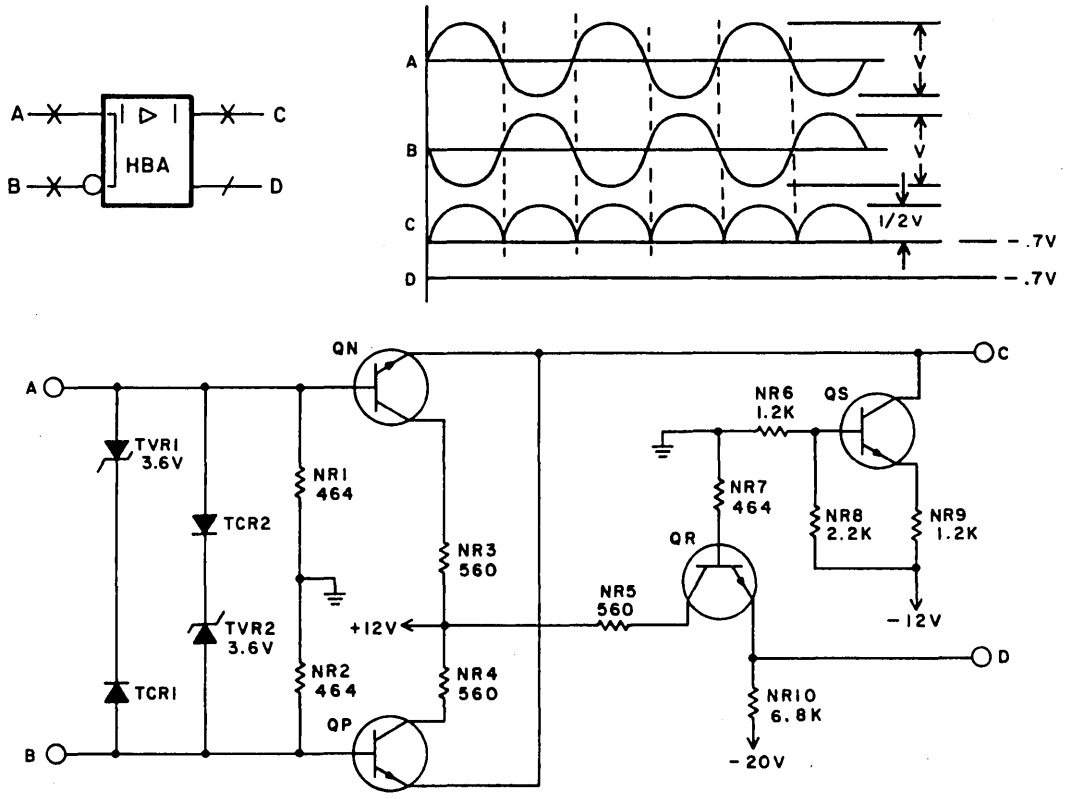
The HBA circuit performs full wave rectification on a differential input signal.

The rectifier consists of QN and QP (matched transistors in an IC array) which are base biased at ground potential by NR1 and NR2. With no signal input, point C rests at -.7 volts. NR6, NR8, NR9, and QS form a current sink network which provides the collector-emitter current for QN and QP.

When a differential input signal (amplified read head output) is present at A and B,the rectification action of QN and QP cause the alternating positive halves to appear at point C (waveform C).

Network NR5, NR7, NR10, and QR set up a DC reference voltage at point D which matches the "no signal" DC voltage at point C (QN, QP, and QR are an IC transistor array).

TCR1, TVR1, TCR2, and TVR2 form a voltage clipping network to prevent overvoltage damage to reverse biased base-emitter junctions of QN and QP.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7JI04A

RECTIFIER - HBB

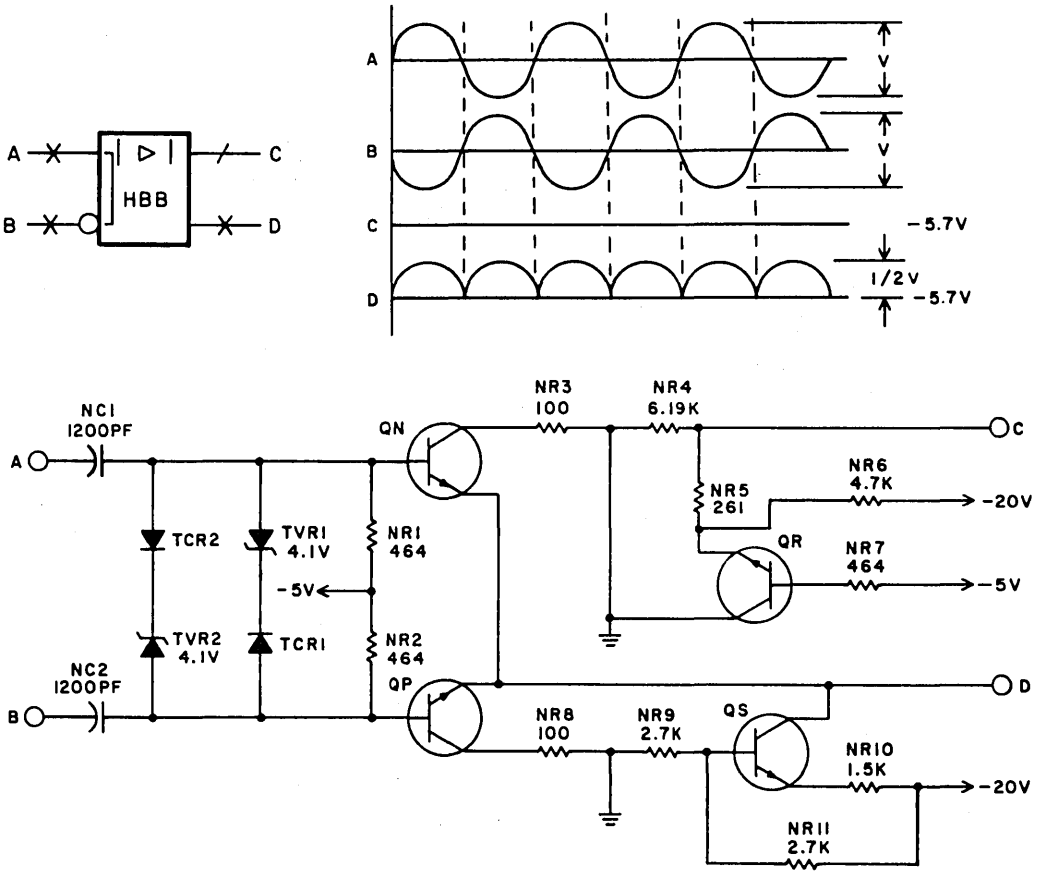
The HBB circuit performs full wave rectification on a differential input signal.

The rectifier consists of QN and QP (matched transistors in an IC array) which are base biased at -5 volts by NR1 and NR2. With no signal input, point D rests at -5.7 volts. NR9, NR10, NR11, and QS form a current sink network which provides the collector-emitter current for QN and QP.

When a differential input signal (amplified read head output) is present at A and B, the rectification action of QN and QP cause the alternating positive halves to appear at point D (waveform D).

Network NR4, NR5, NR6, NR7, and QR set up a DC reference voltage at point C which proportionally tracks the "no signal" DC voltage at point D (QN, QP and QR are an IC transistor array).

TCR1, TVR1, TCR2, and TVR2 form a voltage clipping network to prevent overvoltage damage to reverse biased base-emitter junctions of QN and QP.



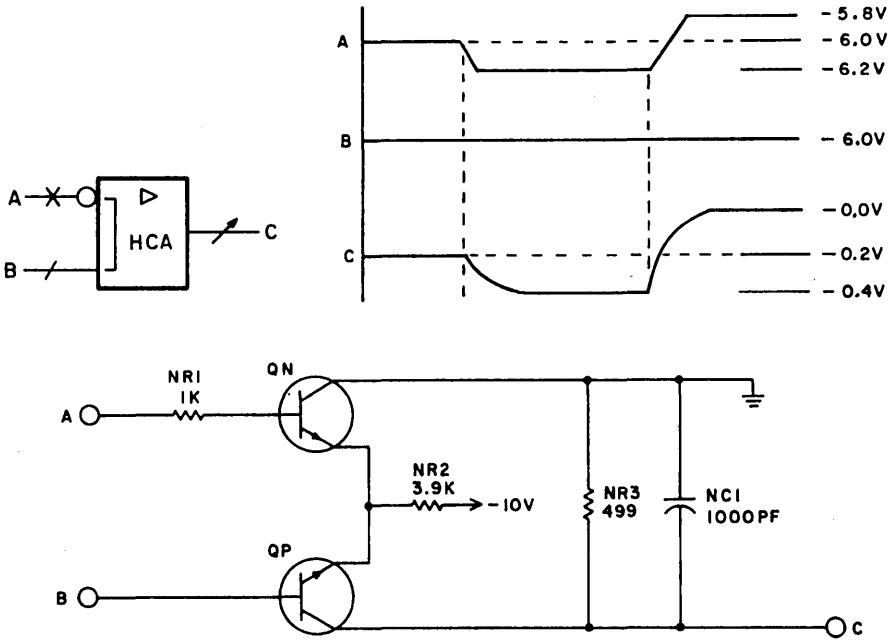
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J103A

DIFFERENTIAL AMPLIFIER - HCA

The HCA circuit is a differential amplifier which is used as a control element in an AGC amplifier feedback loop.

Input B is connected to a fixed reference voltage and input A is connected to an integrated DC voltage which is proportional to the output amplitude of an AGC amplifier. When the voltage on input A is greater than that at input B, the current from emitter resistor NR2 goes through QN to ground. When the voltage on input A is less than at B, the current from NR2 goes through QP to output C. When input A equals input B, the current from NR2 is split between QN and QP. The voltage at point C is established by the current through QP times resistor NR3. Point C is the control voltage input for input E on the HCU (AGC amplifier) circuit. NC1 is used as an integrator and helps stabilize the response time.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J101

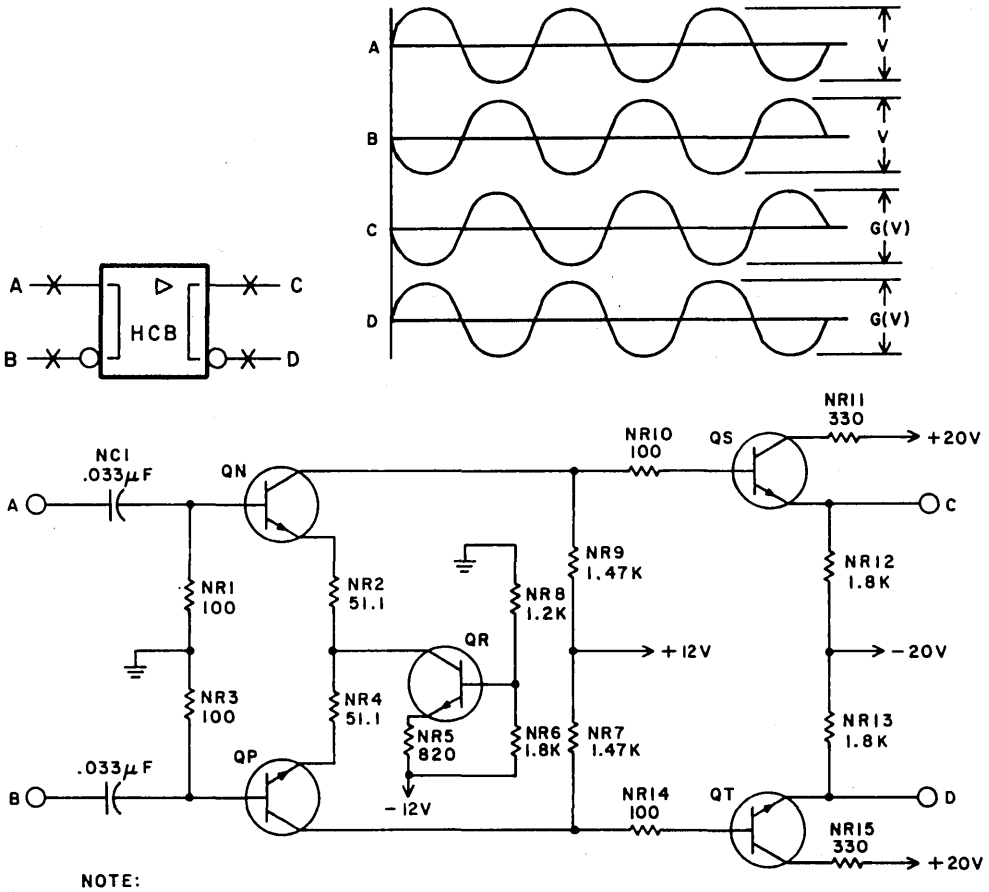
DIFFERENTIAL AMPLIFIER - HCB

The HCB circuit is a single stage differential input, differential output amplifier.

QN and QP are the amplifying transistors. The gain of the amplifier is largely determined by the ratio of NR9 to NR2 and NR7 to NR4.

QR, NR5, NR6, and NR8 are a current sink network which provides collector current for QN and QP.

QS and QT with emitter resistors NR12 and NR13 are emitter followers for low impedance outputs.



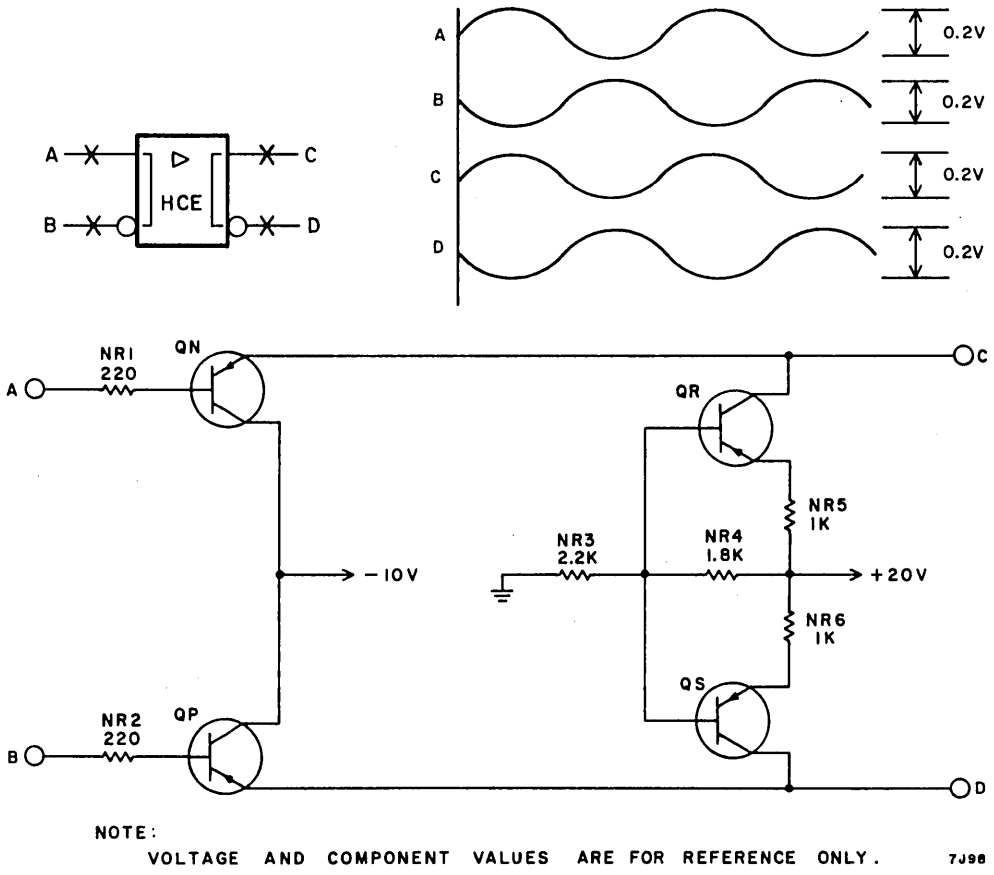
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7 J97

BUFFER AMPLIFIER - HCE

The HCE circuit is a differential buffer amplifier with a gain of approximately one. With the proper bias conditions, inputs A and B can be connected to a circuit such as a differential amplifier output. The effect would be to increase its load driving capabilities without adversely loading down the output signal.

Emitter followers QN and QP present comparatively high input impedance at A and B, and low output impedance at C and D. Current sources QR and QS with NR3, NR4, NR5, and NR6 supply constant emitter current to QN and QP.

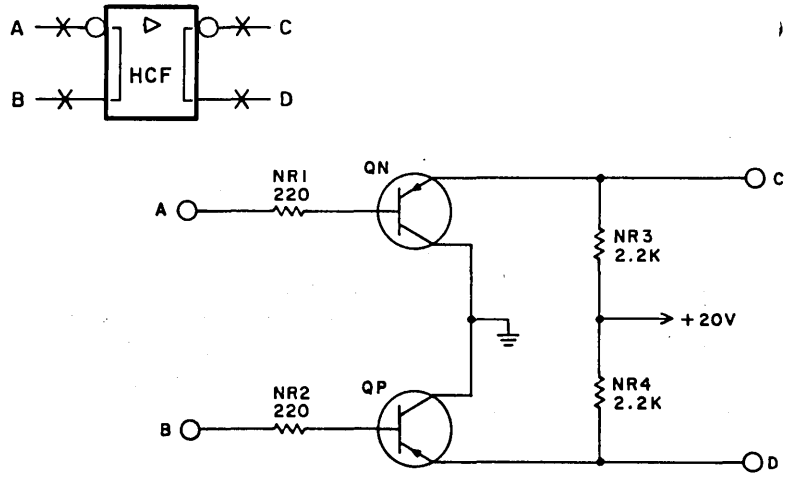


NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J98

BUFFER AMPLIFIER - HCF

The HCF circuit is a differential buffer amplifier with a gain of approximately one. With the proper bias conditions, inputs A and B can be connected to a circuit such as a differential amplifier output. The effect would be to increase its load driving capabilities without adversely loading down the output signal.

QN and QP are emitter followers which present comparatively high input impedance at A and B, and low output impedance at C and D.



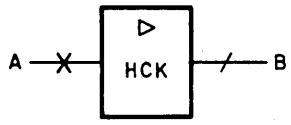
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

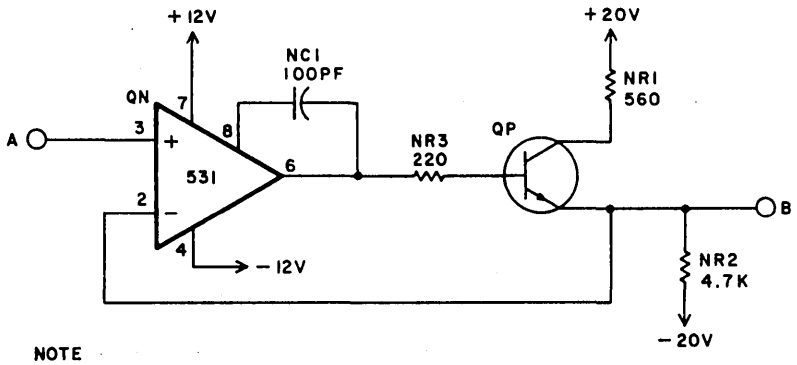
7J95

VOLTAGE FOLLOWER - HCK

The HCK circuit consists of an operational amplifier in a voltage follower configuration. An NPN emitter follower (QP) is enclosed in the feedback loop to provide a voltage output at B equal to the input at A with increased current handling capabilities. Enclosing QP in the feedback loop also negates the change in output due to temperature related voltage variations of the base-emitter junctions of QP.

NR2 provides a minimum load current for QP under no output load conditions. NR1 is a current limit resistor. Resistor NR3 and capacitor NR1 stabilize the circuit.



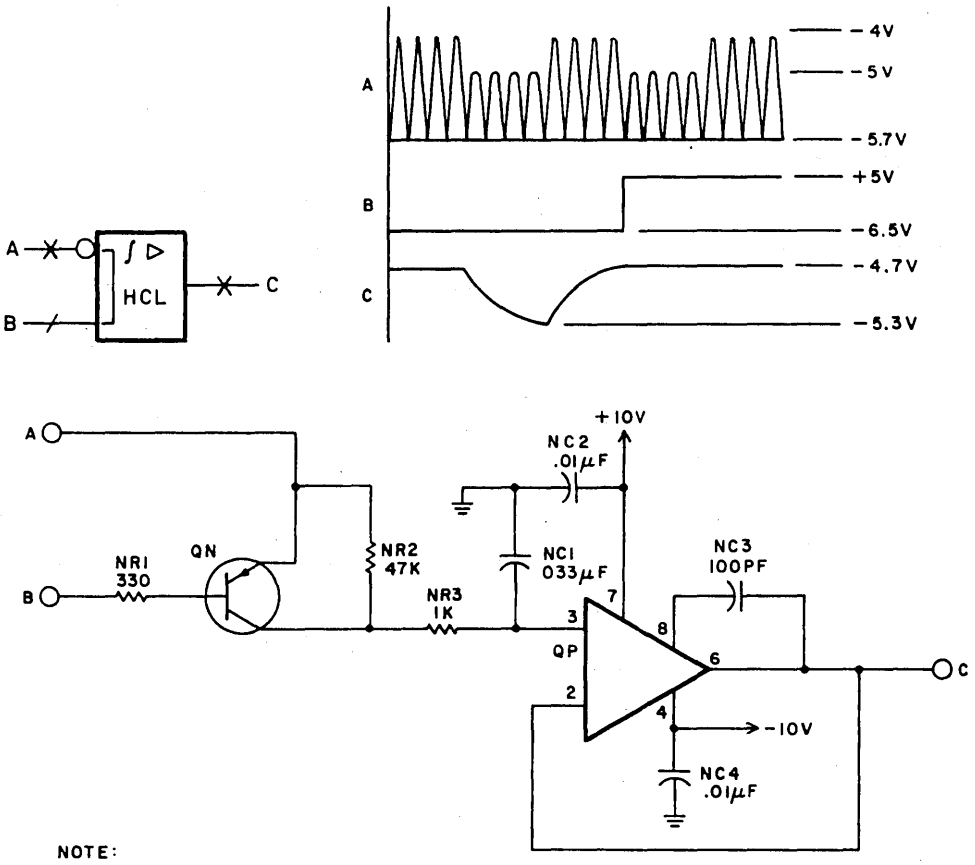


NOTE
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J105

INTEGRATING AMPLIFIER - HCL

The HCL circuit converts a rectified signal input to a DC output that is an average value of the input signal waveform.

The integrating elements are NR2, NR3, and NC1. The analog signal (rectified waveform) is entered at input A. With digital voltage control at input B, QN can be turned on which would bypass NR2. This would leave (NR3) X (NC1) to determine the relatively short response time of the integrator. When QN is turned off, NR2 is included in the integrating circuit and the (NR2 + NR3) X (NC1) long response time results. QP (element 531) is an operational amplifier connected in a voltage follower mode of operation and acts as a buffer amplifier. NC3 is a compensation capacitor for QP.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J102

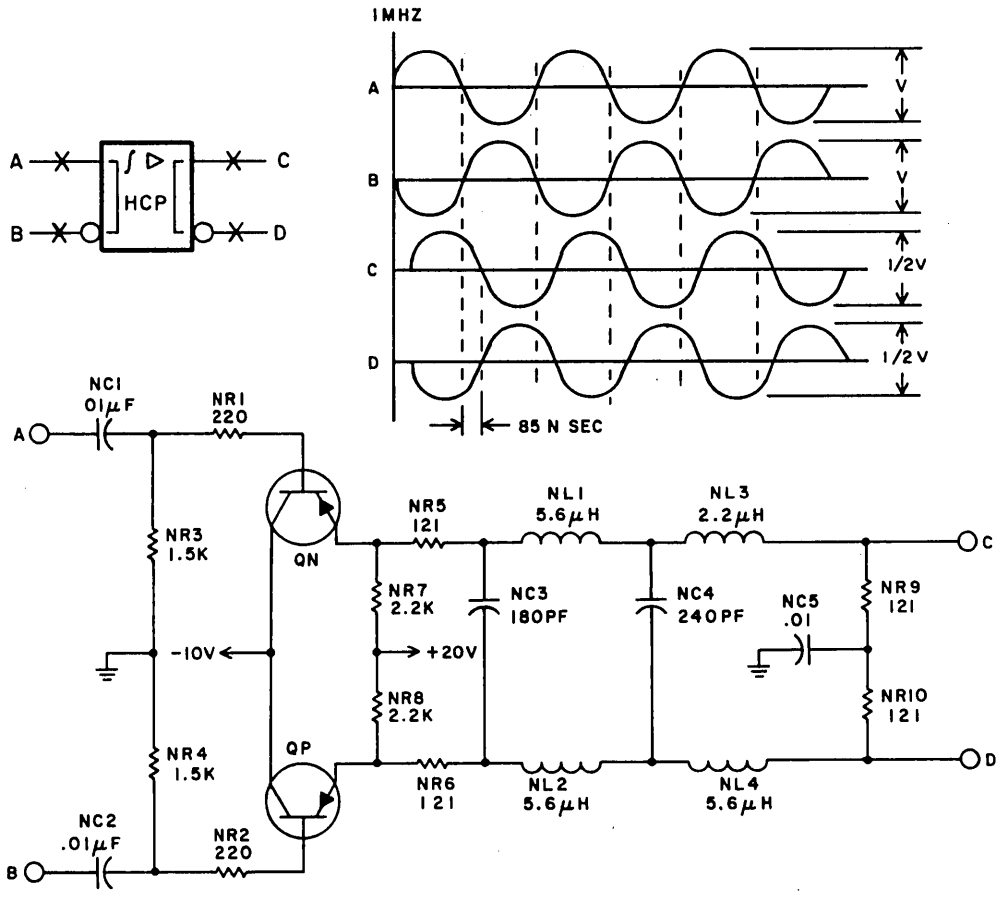
LOW PASS FILTER - HCP

The HCP circuit is a low pass differential filter with a buffer amplifier input (emitter followers). The filter provides attenuation of high unwanted frequencies (noise) in the read back signal with a linear phase response over the frequencies concerning read data.

NL1, NL2, NC3, NC4, NL3, and NL4 make up the differential filter with outputs at C and D. NR9 and NR10 are terminating (impedance-matching) resistors for the filter. NR5 and NR6 are impedance matching resistors to the input of the filter.

QN and QP with their emitter and base resistors form the buffer amplifiers for driving the relatively low input impedance filter.

The upper cutoff frequency of the filter is approximately 5.5 MHz (media compatible data rate of 6.44 MHz). The signal attenuation from inputs A, B, to outputs C, D is about 50% at 1 MHz.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J106

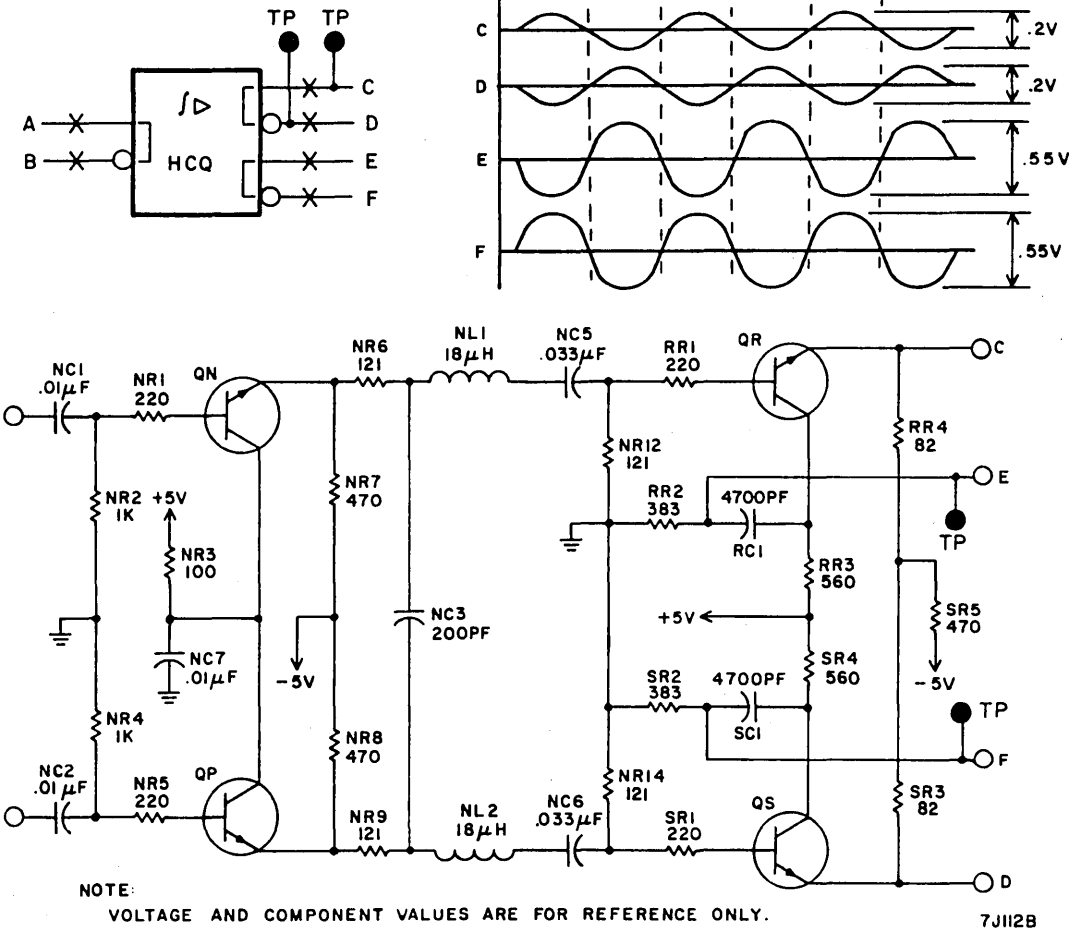
FILTER AND AMPLIFIER - HCQ

The HCQ circuit is a differential, 2 pole low pass filter followed by a differential amplifier with a gain of approximately 2.5.

NL1, NC3, and NL2 make up the 2 pole low pass filter. The upper cutoff frequency is approximately 2.5 MHz for media compatible data rate (6.44 MHz). NR6, NR9, NR12, and NR14 are impedance matching resistors for the filter.

QN and QP are buffer amplifiers (emitter followers) for driving the relatively low impedance filter.

QR, QS, and their associated circuitry perform dual roles as differential buffer amplifiers (emitter followers) and as differential amplifiers. Outputs C and D are the buffered outputs that connect to level detection circuitry with further amplification. Outputs E and F are amplified outputs which connect to a zero cross network (low resolution channel). This signal channel is amplified to make up for the attenuation loss of the filter. The gain of the amplifier is largely determined by the ratio of RR2//RR3 to RR4 and SR2//SR4 to SR3.



AGC AMPLIFIER - HCU

The HCU circuit is a differential amplifier with gain controlled by a negative voltage at input E.

QP and QR are amplifying transistors with their maximum gain determined by the ratio of NR10 to NR5 and NR11 to NR4.

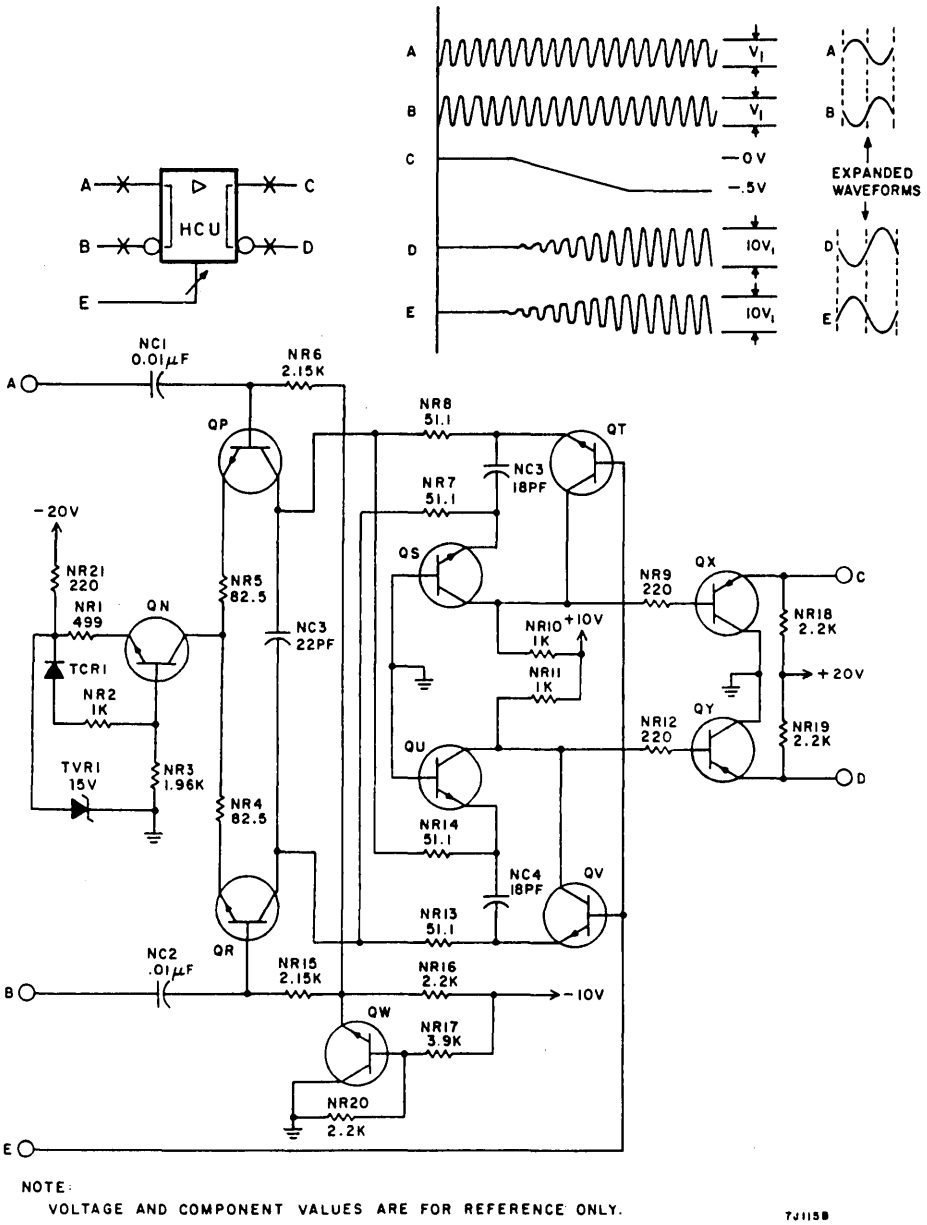
Common base amplifiers, QS, QT, QU, and QV pass amplified current signals to resistors NR10 and NR11. QS and QT pass out of phase signals to collector resistor NR10. Likewise, QU and QV pass out of phase signals to collector resistor NR11.

Control voltages on the bases of QT and QV control circuit gain. With 0 volts for control voltage, QS, QT, QU, and QV turn on equally, causing out of phase voltage to cancel, leaving a net output or gain of 0 volts. Increasing the control voltage negatively starts turning off QT and QV causing the amplifier gain to increase. Turning off QS, QT, QU, and QV requires that the control voltage be approximately -0.5 volts, which allows an amplifier gain of 10.

Emitter followers QX and QY provide low output impedance.

QN, NR1, NR2, NR3, and TCR1 make up a current sink network which controls the collector current of QP and QR.

NR21 and TVR1 form a -15 volt regulated voltage for the current sink circuit.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J1158

HJM

Information not available at time of printing. It will be supplied at a later revision.

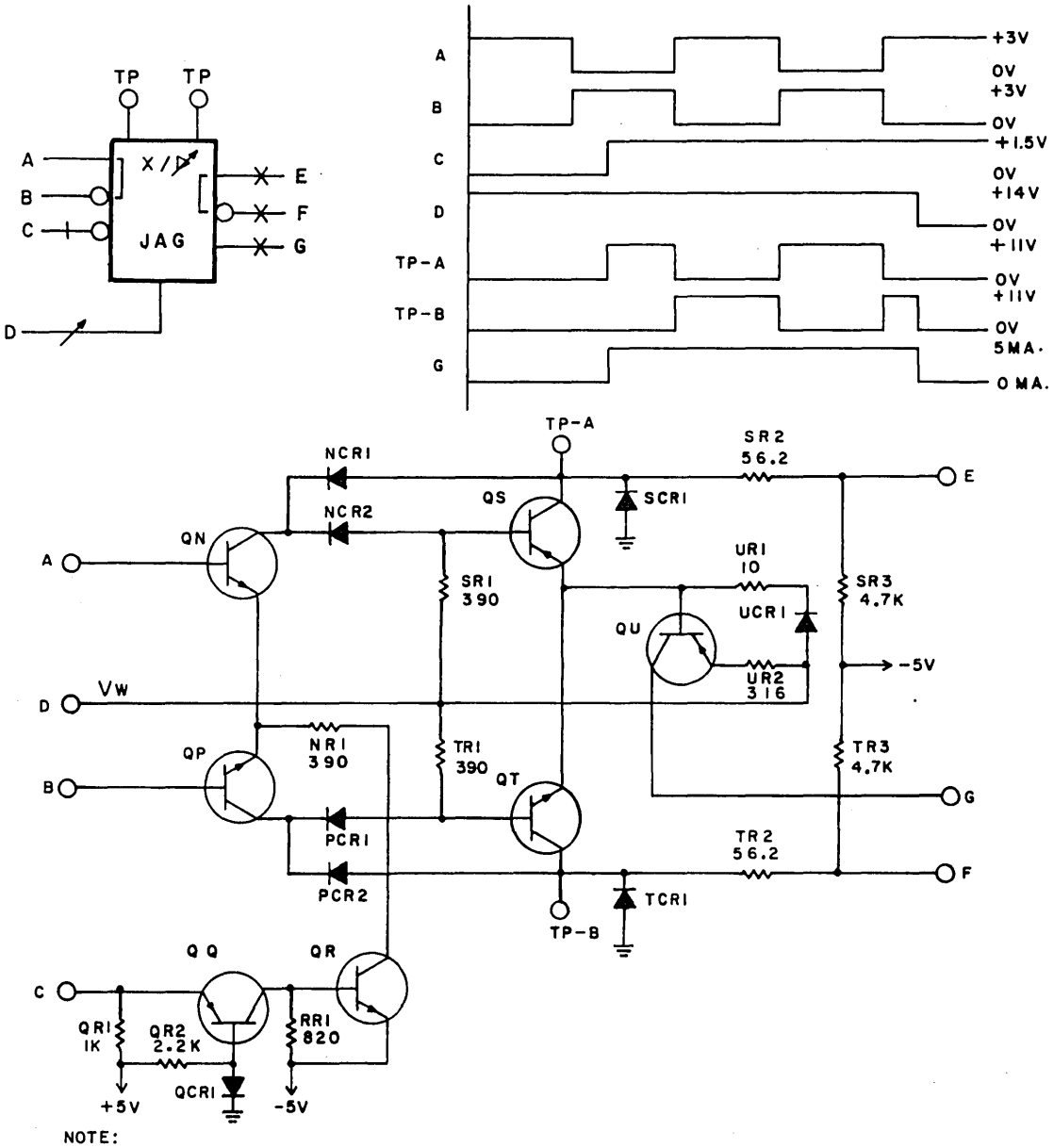
ICD

Information not available at time of printing
It will be supplied at a later revision.

WRITE DRIVER - JAG

Write driver JAG is a differential voltage switch which converts voltage (across termination resistors) to current to drive a differential recording head.

Circuit operation is dependent upon signal level shifter QQ converting an open collector TTL output of "0" or "1" to turning QR "off" and "on". With QR on, -5 volts flows through QR and NR1 to supply current for the differential switches QN and QP. With input A high and B low, QN turns on and QP is off. QN turning on causes QS to turn on which applies a voltage (from D through UCR1 and UR1) to termination resistor SR2 and current to output E. When A is low and B is high QN and QS turn off, QP and QT turn on applying voltage to termination resistor TR2 and current to output F. Current sensing network UR1, UR2, UCR1 and QU supply current at G which is used for fault detection. NCR1, NCR2, PCR1, PCR2 prevent QS and QT from saturating when the write driver is turned off. SCR1, SR3, TCR1, and TR3 provide back biasing of the write matrix diodes during a write operation.



NOTE:

1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
2. WAVEFORMS ABOVE ARE FOR REFERENCE ONLY AND VALID ONLY WHEN OUTPUTS E AND F ARE CONNECTED TO A READ/WRITE HEAD WITH CENTER TAP TO GROUND.

7J26

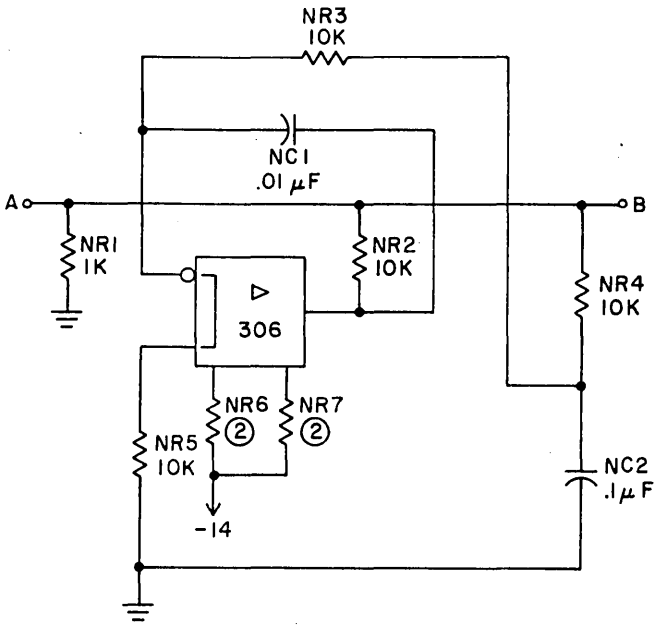
JAL

Information not available at time of printing. It will be supplied at a later revision.

AUTO NULL CIRCUIT - JAM

The JAM circuit provides a DC null for the AC signal on line AB. This circuit compensates for a fluctuation in DC reference of the AC signal due to temperature and chip-to-chip parameters.

The operational amplifier senses the DC level on line AB and compares this voltage level against a zero volt reference. It then supplies the proper DC current to maintain a DC null on line AB.



NOTES:

1 VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

② VALUES CHOSEN PER CIRCUIT REQUIREMENTS.

7J199

LCI

Information not available at time of printing. It will be supplied at a later revision.

VOLTAGE CONTROLLED OSCILLATOR - MAF/MAH

The MAF/MAH circuit consists of two Schmitt trigger circuits (QQ, QR and QS, QT) and a differential switch/current limiter circuit (QN, QP, NR1, and NR2). The values of capacitor PC1, resistors NR1 and NR2, and the input voltage, determines the output frequency of the circuit. Operating frequency is listed on the Logic Diagram (see Section 5).

For the following discussion, assume that voltage E3 is more positive than E2, E2 is more positive than E1, and E0 is the lowest voltage (refer to Figure 1).

Assume that point C of PC1 is more positive than point D. At this time, QP and QS are both conducting and QT is off (base-emitter junction is reverse biased). The output voltage at B is high. The other half of the circuit (QN, QQ, and QR) is in the opposite state at this time.

The D terminal of capacitor PC1 is held low by the forward drop of the base-emitter junction of QR. Therefore, current through PC1 alters its charge linearly until the voltage at C reaches the high output voltage. At this point, the lower Schmitt trigger circuit (QS, QT) switches off and the output voltage at B goes to ground. QP now switches off and point C is driven rapidly positive by the forward biased base-emitter junction of QS.

At the instant that the lower Schmitt trigger circuit switched off, the voltage at point D was at E3. The sudden increase of point D to E3 potential reverse biases the base-emitter junction of QR and triggers the upper Schmitt trigger circuit. Therefore, QN and QQ turn on and draw current from terminal D of capacitor PC1. When the voltage at D reaches E1, the upper Schmitt trigger circuit switches off. QN switches off and point C is again raised to E3. This completes the multivibrator cycle and brings it back to the initial condition. The cycle is then repeated.

As input A becomes more negative and output frequency at B, increases linearly (refer to Figure 2).

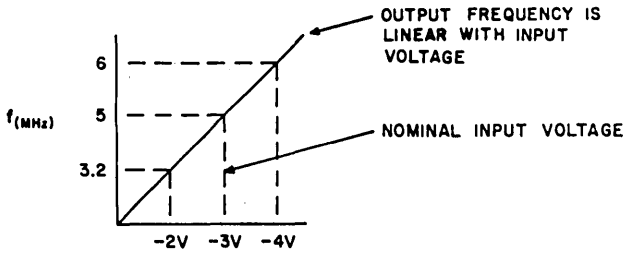


Figure 2

Diode PCR3 prevents the emitters of QN and QP from falling to a voltage that would cause both transistors to conduct when power is first applied. Such a condition would prevent the circuit from oscillating. Diodes QCR1, RCR1, SCR1, and TCR1 prevent the Schmitt transistors (QQ, QR,QS, and QT) from going into full saturation. This helps the circuit to oscillate at the higher frequencies.

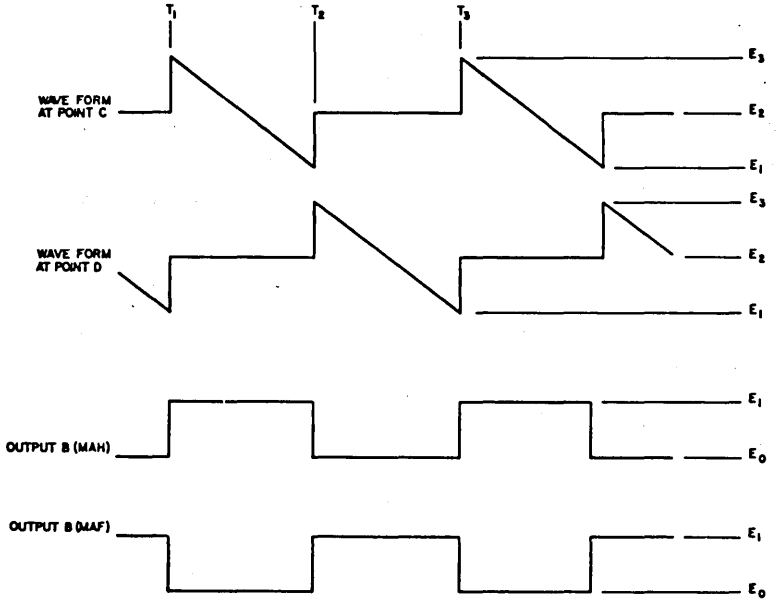
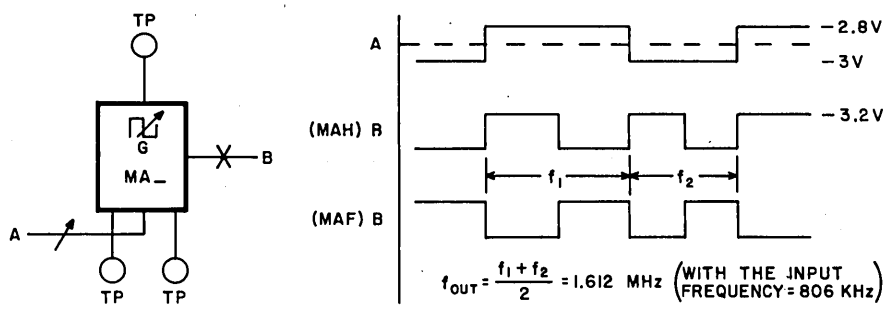
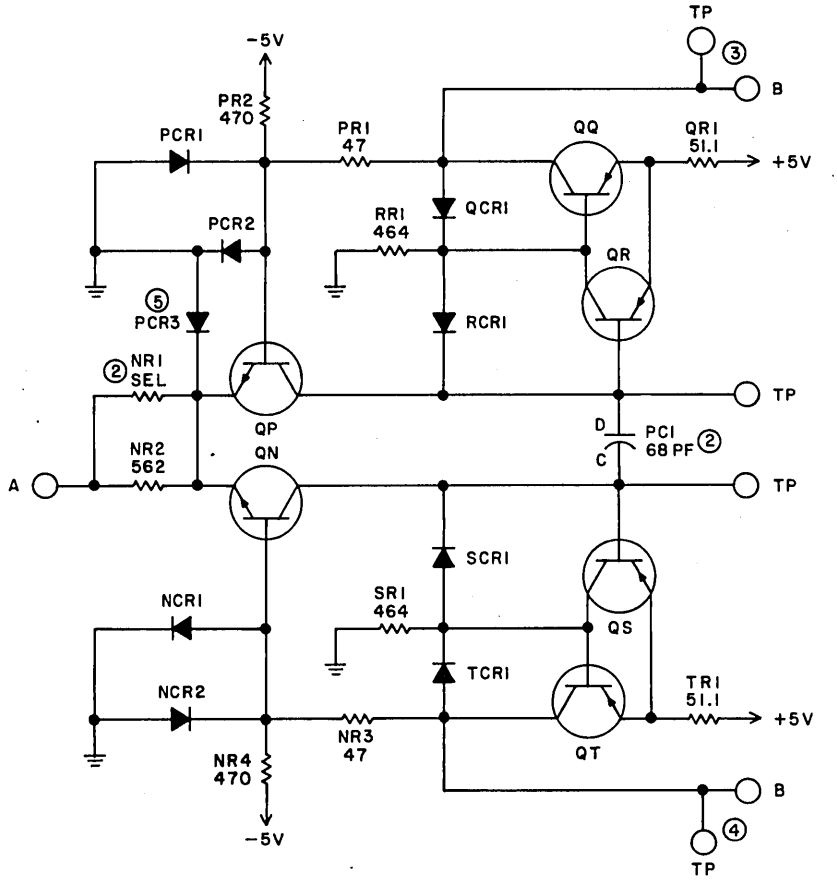


Figure 1





NOTES:

1. VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
2. VARIES WITH DATA FREQUENCY. THESE COMPONENTS CONTROL FREQUENCY.
3. OUTPUT LOCATED ON MAH CIRCUIT.
4. OUTPUT LOCATED ON MAF CIRCUIT.
5. DIODE PCR3 ON MAH ONLY.

7J28A

SPEED DETECTOR - QDE

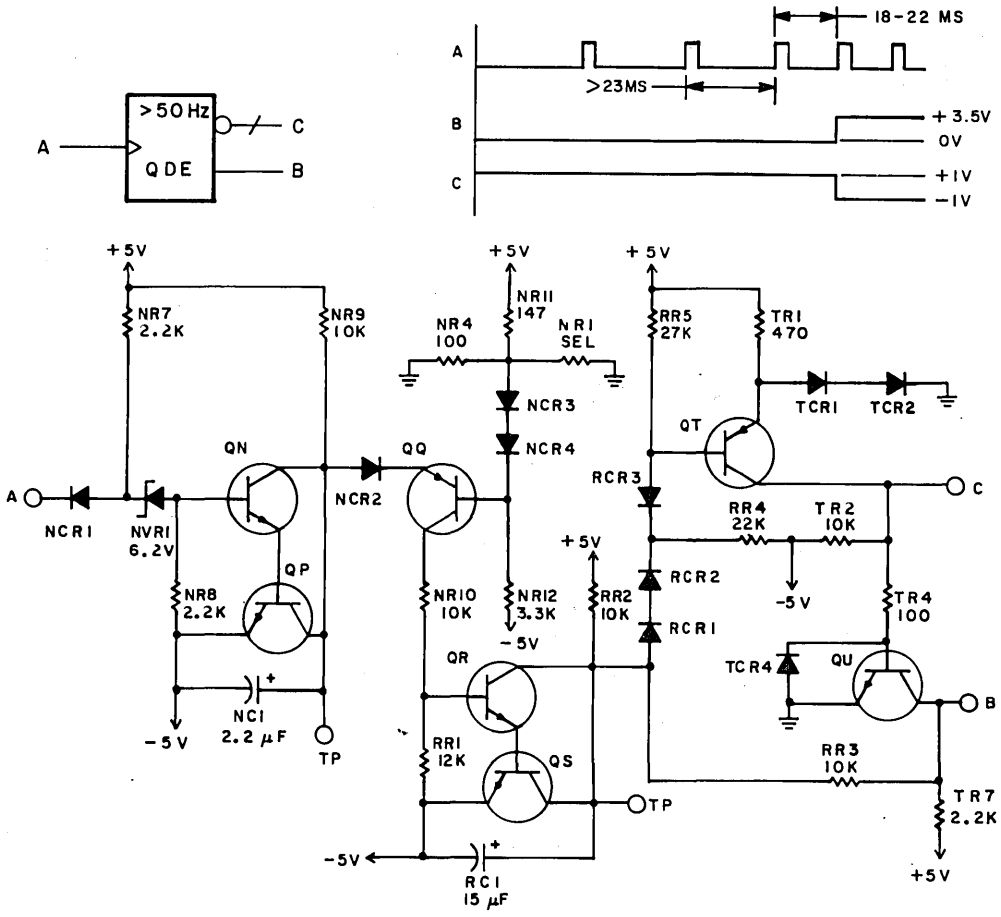
The QDE circuit monitors the sector pulses to determine whether or not the spindle is at a specified speed.

Each time a sector is sensed, a 55-µsec pulse appears at input A. Transistors QN and QP conduct and completely discharge capacitor NC1 to -5v. When the pulse drops, NC1 begins charging through NR9. When the voltage on the collectors of QN and QP reaches the threshold of NCR2 and QQ, QQ turns on. This causes transistors QR and QS to conduct and discharge RC1. With QR and QS on, RCR1 and RCR2 are back biased and the voltage at the base of QT drops, turning QT on. The collector voltage of QT rises enough to turn QU on and the output voltage at B goes low to indicate a not up to speed condition.

If the disk pack is below speed, pulses at input A are at low repetition rate. Capacitor NC1 discharges and charges turning transistors QQ, QR, and QS off and on, respectively. This in turn causes RC1 to charge and discharge. Every time NC1 charges to the threshold, QQ, QR, and QS turn on and discharge RC1. This prevents RCR1 and RCR2 from ever becoming forward biased. As a result, QT remains on and the output at B remains low, indicating not up to speed.

When the disk pack reaches the required speed, the charging time of NC1 is such that the charging voltage on NC1 remains below the threshold of NCR2 and QQ, keeping QQ,QR, and QS off. Now RC1 has time to charge and when RCR1 and RCR2 become forward biased,the voltage at the base of QT increases sufficiently for QT to turn off. The resulting reverse bias on QU turns QU off and the output at B goes high. The feedback through RR3 reduces the charge time of RC1 and the switchover goes to completion with the high output at B indicating an up to speed condition. The output signal at C is always complementary and is used by a relay driver circuit.

The voltage on the base of QQ is determined by the voltage divider comprised of NR1,NR4, NR11,NR12,NCR3, and NCR4. Resistor NR1 is a test selected resistor to fine tune the threshold of NCR2 and QQ and to compensate for the tolerances of NR9 and NC1.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J29

VOLTAGE CHECKER - QEH

The QEH circuit detects decreases in power supply voltages that are beyond a specified level. A fault condition (output C equals "0") occurs if:

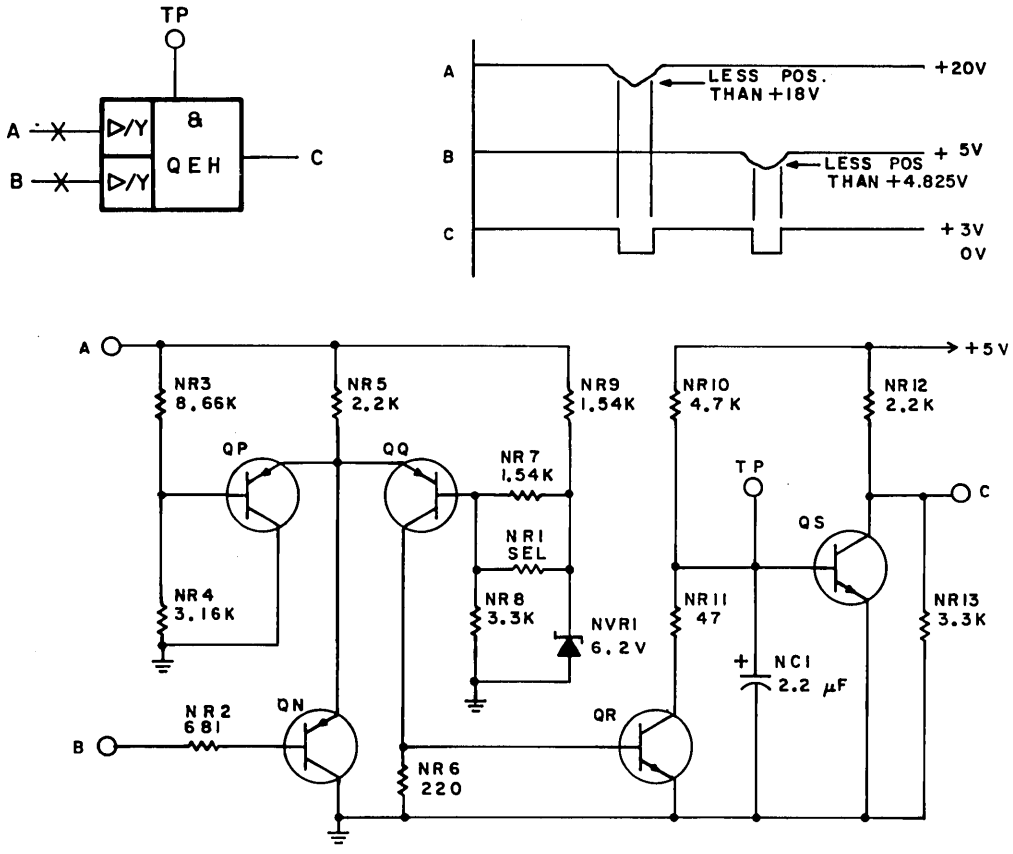
1. +5 volt supply becomes less positive than +4.825 volts, or

2. +20 volt supply becomes less positive than +18.0 volts.

The base voltage at transistor QQ is determined by zener diode NVR1 and a voltage divider network (NR7, NR8, NR9, and NR1). This base voltage is established at +4.825 volts. If the positive supplies connected to inputs A and B are normal, QP and QN are off and transistor QQ is on. The resulting positive level at the collector of QQ turns on transistor QR. This causes the collector of QR to drop the near zero volts switching QS off and establishing a +3 volt level at output C.

Transistors QN and QQ operate on each other as a comparator. When the base voltage on QN becomes less positive than the base voltage on QQ (+4.825 volts), QN turns on and QQ turns off. With the base of transistor QR at zero volts, transistor QR turns off pulling the base of QS positive and turning it on. As a result, output C approaches a level near zero volts.

Transistors QP and QQ also operate on each other as a comparator. The voltage divider, composed of resistors NR3 and NR4, is sized so that when the +20 volt input at A goes less positive than +18 volts, transistor QP turns on and output C goes low.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J30

VOLTAGE CHECKER - QEJ

The QEJ circuit detects decreases in power supply voltages that are beyond a specified level. A fault condition (output C equals "0") occurs if:

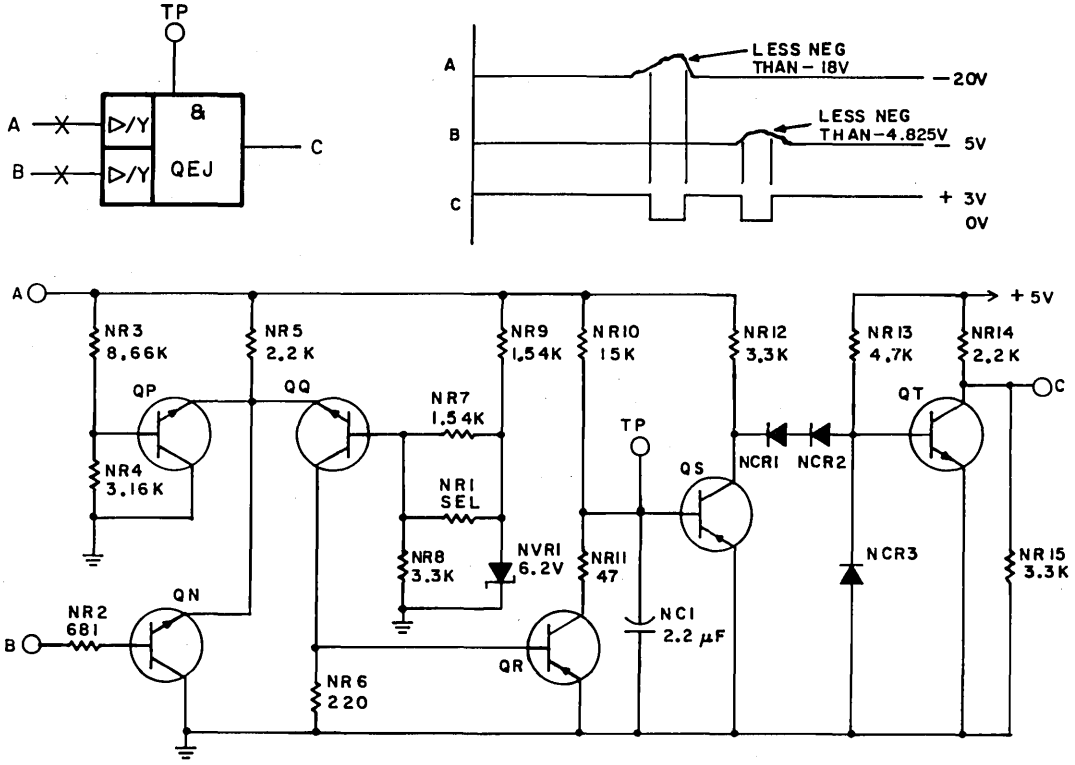
1. -5 volt supply becomes less negative than -4.825 volts, or

2. -20 volt supply becomes less negative than -18.0 volts.

The base voltage at transistor QQ is determined by zener diode NVR1 and a voltage divider network (NR7, NR8, NR9, and NR1). This base voltage is established at -4.825 volts. If the negative supplies connected to inputs A and B are normal, QP and QN are off and transistor QQ is on. The resulting negative level at the collector of QQ turns on transistor QR. This causes the collector of QR to drop to near zero volts switching QS off and developing a reverse bias across diode NCR3. This turns off transistor QT and sets the output at C to +3 volts.

Transistors QN and QQ operate on each other as a comparator. When the base voltage on QN becomes less negative than the base voltage on QQ (-4.825 volts), QN turns on and QQ turns off. With the base of transistor QR at zero volts, transistor QR turns off pulling the base of QS negative and turning it on. Diodes NCR1 and NCR2 raise the base voltage of transistor QT to a point where it turns on and causes output C to approach a level near zero volts.

Transistors QP and QQ also operate on each other as a comparator. The voltage divider, composed of resistors NR3 and NR4, is sized so that when the -20 volt input at A goes less negative than -18 volts, transistor QP turns on and output C goes low.



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J31

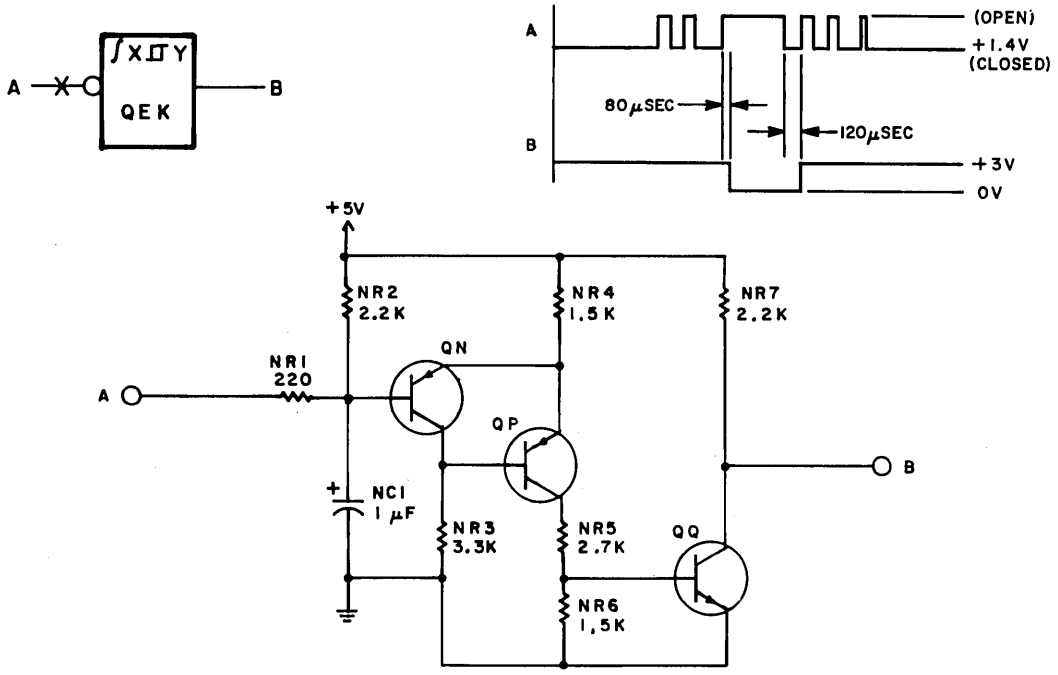
SWITCH RECEIVER - QEK

The QEK circuit produces a "1" (+3v) output at B when the solid-state switch connected to input A is closed. When the switch is open a "0" (0v) appears at output B.

A transistor switch is connected to input A. When this switch is open, capacitor NC1 approaches +5v and QN turns off. Transistor QP is, therefore, on and conducts current to the base of QQ through resistor NR5. Transistor QQ turns on, conducting current away from output B, and drops the output to near ground or a "0".

When the switch is closed, the voltage flow through NR1, the switch, and across NC1 increases rapidly because of the short time constant of NR1 and NC1. Any spurious switching that precedes the state change increases the discharge time. As the voltage across NC1 decreases, QN begins to turn on. As QN conducts current to the base of QP, the forward bias on QP decreases and QP begins to turn off. As QP turns off, the current through NR4 decreases due to the higher lead resistance (NR3) of QN compared with QP (NR5). The current drop through NR4 causes a decrease in the voltage drop across NR4. The bias on QN is, therefore, increased. The cycle goes rapidly to completion. Transistor QP is turned off. With QP off, the base of QQ is near ground, causing QQ to turn off. This allows the +5v supply to flow through NR7 to output B raising the output to +3v, "1".

When the transistor switch driving the input is not conducting, NC1 charges slowly to +5v due to the long time constant of NR2 and NC1. Again, any preliminary switching that precedes the actual state change will hold NC1 well below the switching level of QN. As the voltage across NC1 increases, QN begins to turn off. Transistor QP begins to conduct current away from the emitter of QN. Transistor QP turns on rapidly because of the positive feedback. The output then becomes "0".



NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J32

SYMMETRY RESTORER - QEL

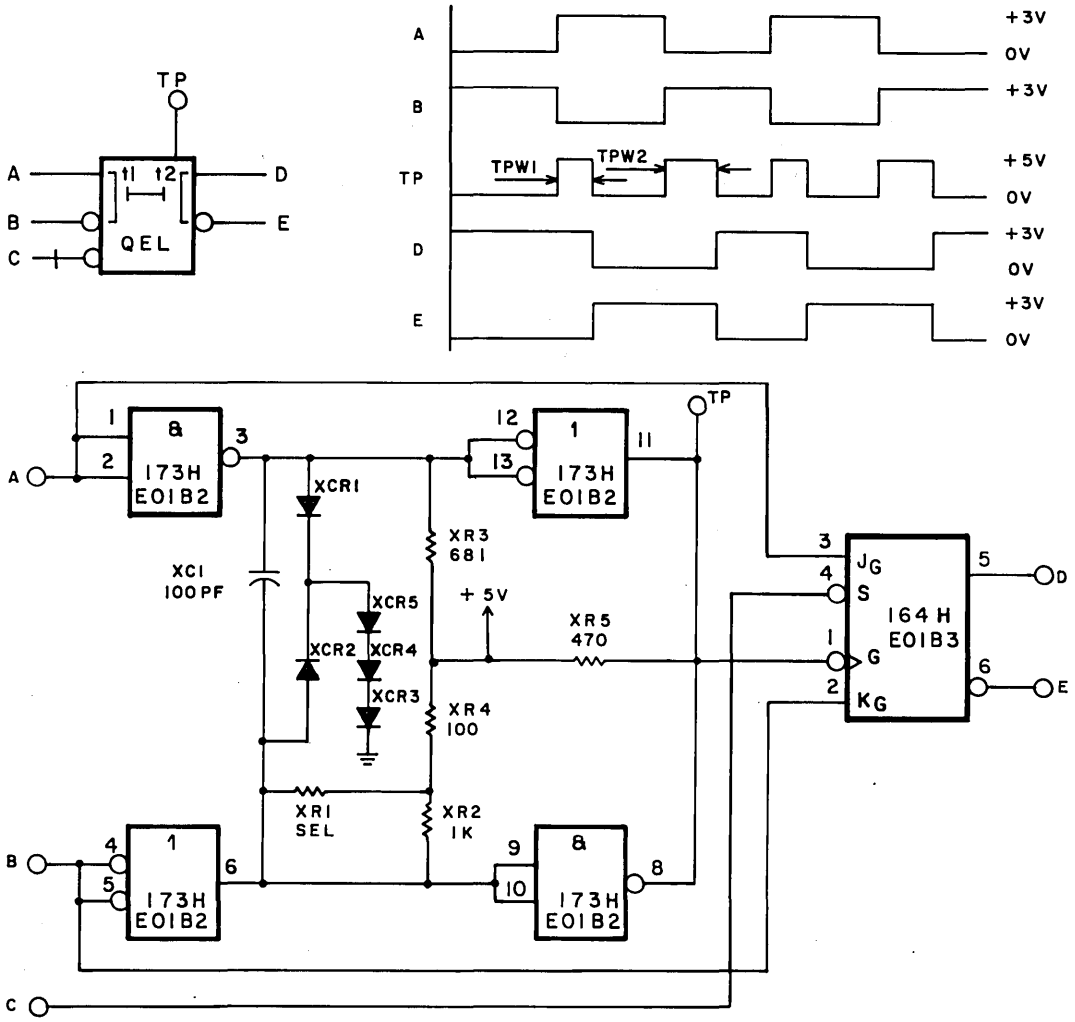
In a write driver chain where complementary TTL input signals become asymmetrical by ±8 nsec, the QEL circuit is used to restore symmetry to these signals.

A "0" TTL level at point C will set the flip-flop ensuring the same start-up conditions on inputs D and E when released by a "1" level at C.

With input A high and B low, pin 3 of 173H goes to ground and pin 6 goes to +5v through XR1, XR2, and XR4. The ground transition at pin 3 is coupled through XC1 and forces a negative spike on pin 6. Starting from a negative potential pin 6 voltage rises toward +5 volts at an RC time rate determined by XC1 and the combination of XR1, XR2, and XR4. This causes the pulse to be delayed in reaching the switching threshold of the following inverter (pins 9 and 10), and produces a positive pulse at "ored" pins 8 and 11 for the duration of the delay. The negative edge of this pulse triggers pin 1 of flip-flop 164H changing the state of outputs D and E.

The opposite conditions on inputs A and B (A low and B high) form the positive pulse at "ored" points 8 and 11 which is determined by the RC combination of XC1 and XC3. Thus, the negative edge which triggers the J-K flip-flop is controlled by alternate RC time constants, one of which can be adjusted by selection of XR1 with reference to the other resistors.

Diodes XCR1, XCR2, XCR3, XCR4, and XCR5 clamp the positive excursion on pins 3 and 6 at +2.5 volts to make delays insensitive to frequency variations up to data rates of 4 MHz.



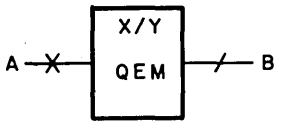
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

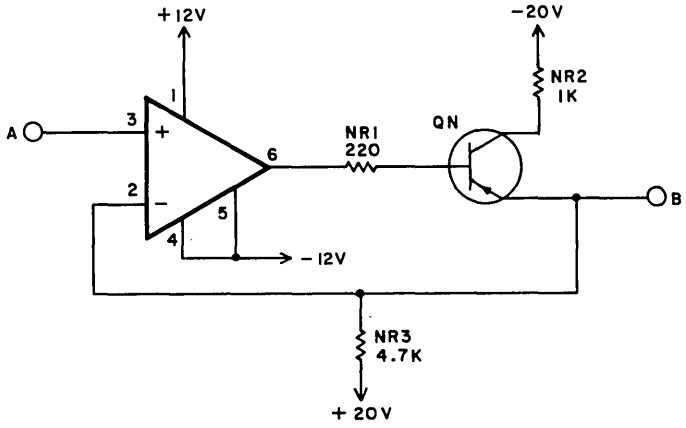
7J33

VOLTAGE FOLLOWER - QEM

The QEM circuit consists of an operational amplifier in a voltage follower configuration. A PNP emitter follower (QN) is enclosed in the feedback loop to provide a voltage output at B equal to the input at A with increased current handling capabilities. Enclosing QN in the feedback loop also negates the change in output due to temperature related voltage variations of the base-emitter junctions of QN.

NR3 provides a minimum current to the emitter of QN under no load conditions. NR2 is a current limit resistor. NR1 is a buffer resistor to eliminate possible oscillation tendencies.





NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

7J100

FUNCTION GENERATOR - QGD

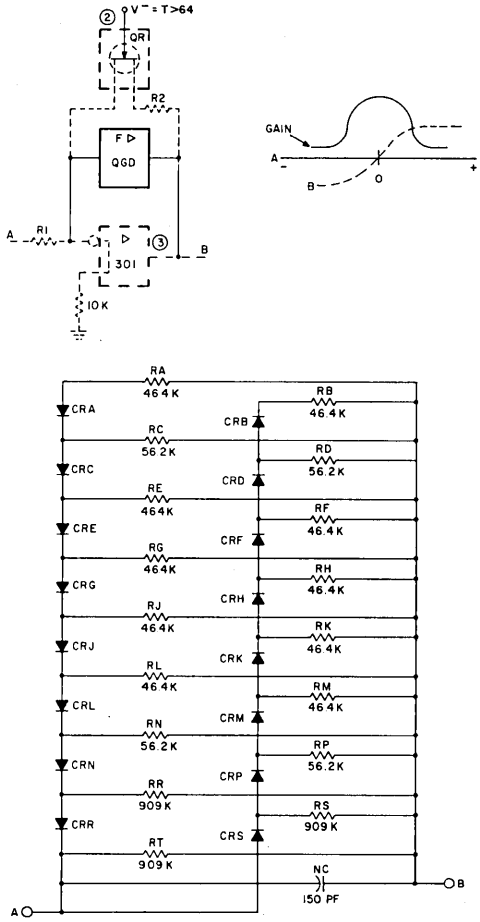
The QGD circuit is a nonlinear feedback network used as the gain determining element of an operational amplifier.

In actual circuit use, the op amp generates a voltage proportional to the desired velocity of the read/write head positioner. The amplitude of this signal is the analog representation of the number of tracks to go (position error) and will be compared with velocity to achieve maximum deceleration control without overshoot of the positioner when on cylinder (T=0).

Field effect transistor QR is part of the GJB circuit to function as a logic switch. Prior to T=64, the input is at ±10 volts with the switch open. With this input voltage, the voltage drops across all of the forward-biased diodes are overcome so that the equivalent resistance of the parallel resistor network in the QGD circuit is about equal to the input resistor R1. The gain is, therefore, unity (output is 10 volts, inverted from input).

When there are less than 64 tracks to go, the input to the gate of QR changes from a negative voltage to ground potential. QR turns on, adding R2 into the feedback loop. R2 has the same resistance as R1. This reduces the feedback resistance to one-half of its former value, thus reducing the gain by 50% (output = ±5 volts).

After T=32, input A begins to decrease in proportion to the remaining position error. The QGD/op amp circuit maintains an output voltage for optimum deceleration. The optimum deceleration is obtained by taking the square root of the position signal and comparing it with the velocity signal. The resistor-diode circuits in the QGD supply the position signal: as the input is reduced, the output is reduced correspondingly. Fewer diodes conduct, removing some of the parallel resistors in the QGD circuit from the feedback loop. This increases the effective feedback resistance, increasing circuit gain. Gain is maximum (but not greater than one) when the output is below about ±0.5 volt.



NOTES: 1 VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.
② PART OF GJB CIRCUIT (REF ONLY). NEG INPUT TURNS QR OFF.
③ SHOWN FOR REFERENCE ONLY.

6TI39A

SWITCH RECEIVER - RCB

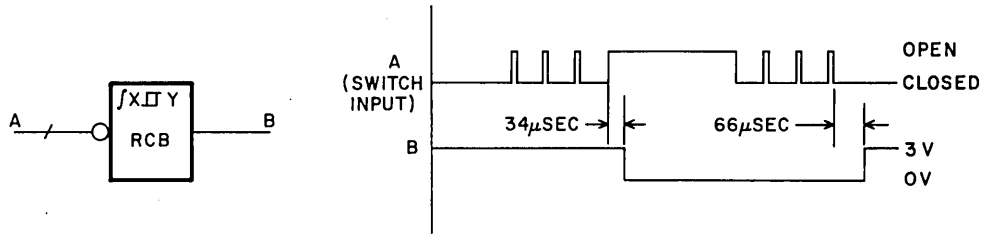
Switch Receiver RCB produces a "1" (+3v) output at B when the grounded switch connected to input A is closed. When the switch is open a "0" (0v) is felt at output B.

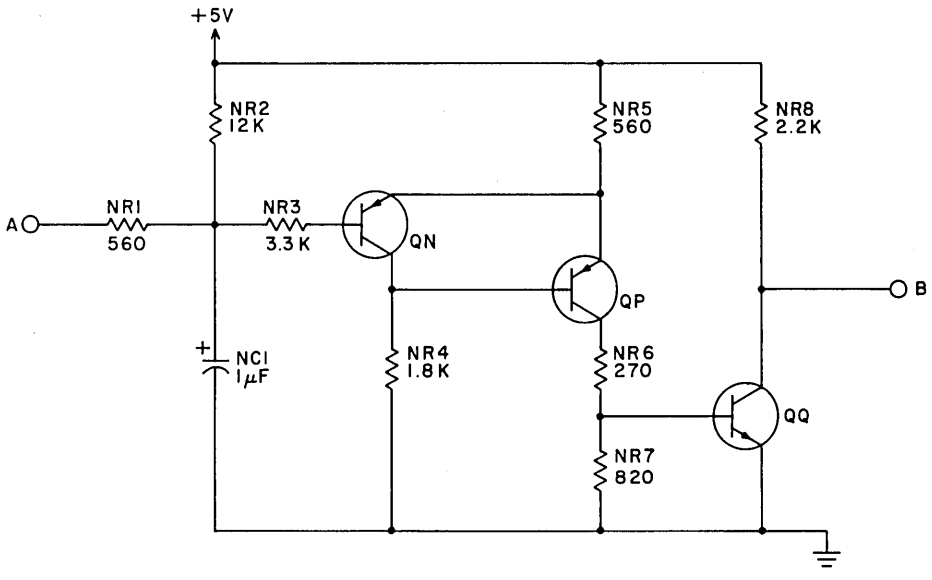
A switch to ground is connected to input A. When this switch is open, capacitor NC1 approaches +5v and QN is shut off. Transistor QP is, therefore, on and conducts current to the base of QQ through resistor NR6. Transistor QQ turns on, conducting current away from output B, and drops the output to near ground or a "0".

When the switch is closed, the voltage across NC1 rapidly increases through NR1 and the switch to ground because of the short time constant of NR1 and NC1. Any contact bounce on the switch will increase the discharge time. As the voltage across NC1 decreases, QN begins to turn on. As QN conducts current to the base of QP, the forward bias on QP is decreased and QP begins to turn off.

As QP turns off, the current through NR5 decreases due to the higher lead resistance (NR4) of QN compared with QP (NR6). The current drop through NR5 causes a decrease in the voltage drop across NR5. The bias on QN is, therefore, increased. The cycle goes rapidly to completion. Transistor QP is shut off. With QP off, the base of QQ is near ground, causing QQ to shut off. This allows the +5v supply to flow through NR8 to output B raising the output to +3v, "1".

When the switch is opened again, NC1 charges slowly to +5v due to the long time constant of NR2 and NC1. Any contact bounce on the switch will hold NC1 well below the switching level of QN until the bouncing ceases. As the voltage across NC1 increases, QN begins to turn off. Transistor QP begins to conduct current away from the emitter of QN. Transistor QP turns on rapidly because of this positive feedback. The output then returns to "0".





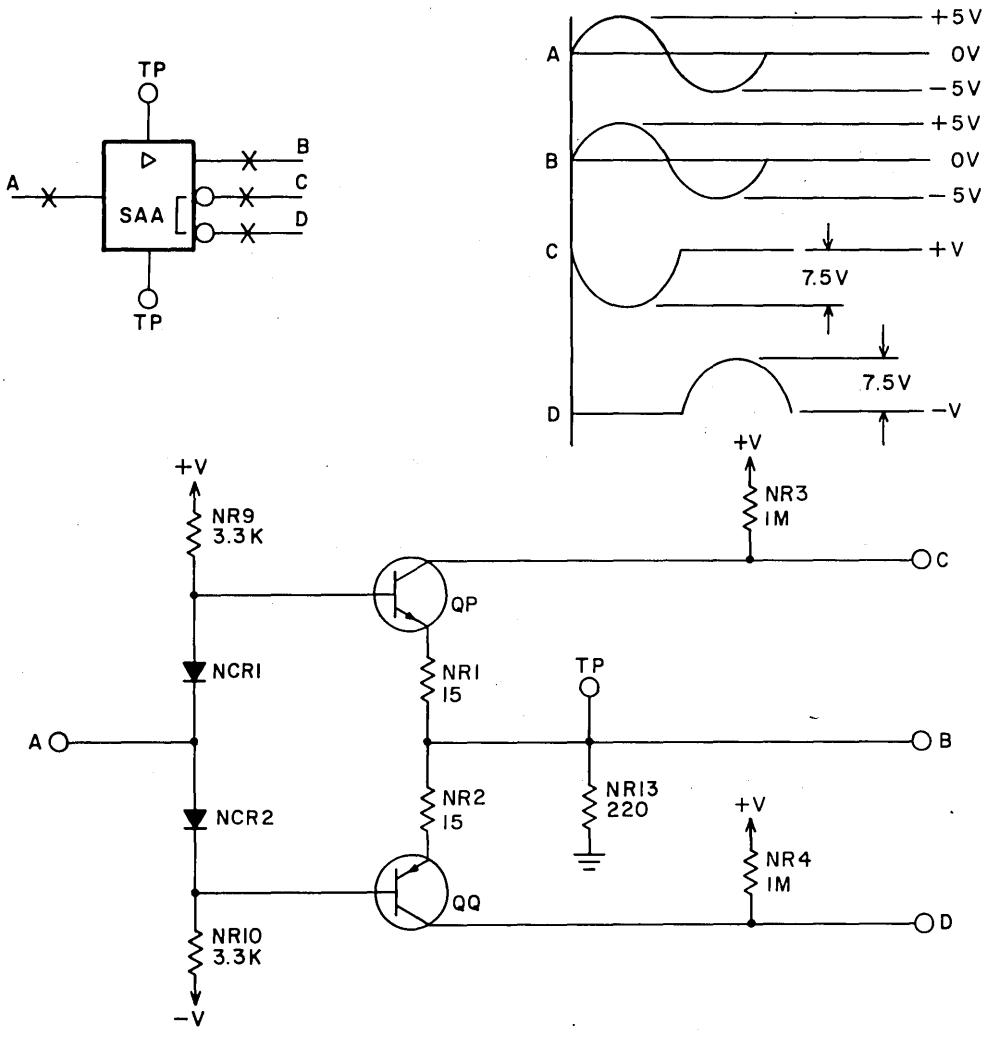
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T145

BIPOLAR CURRENT BUFFER - SAA

The SAA circuit is a power output stage for an operational amplifier. Transistors QP and QQ comprise a complementary output driver and are always biased slightly on by diodes NCR1 and NCR2.

The quiescent current in the output driver is nominally 6.5 ma and the maximum signal amplitude for the circuit is ±5 volts.



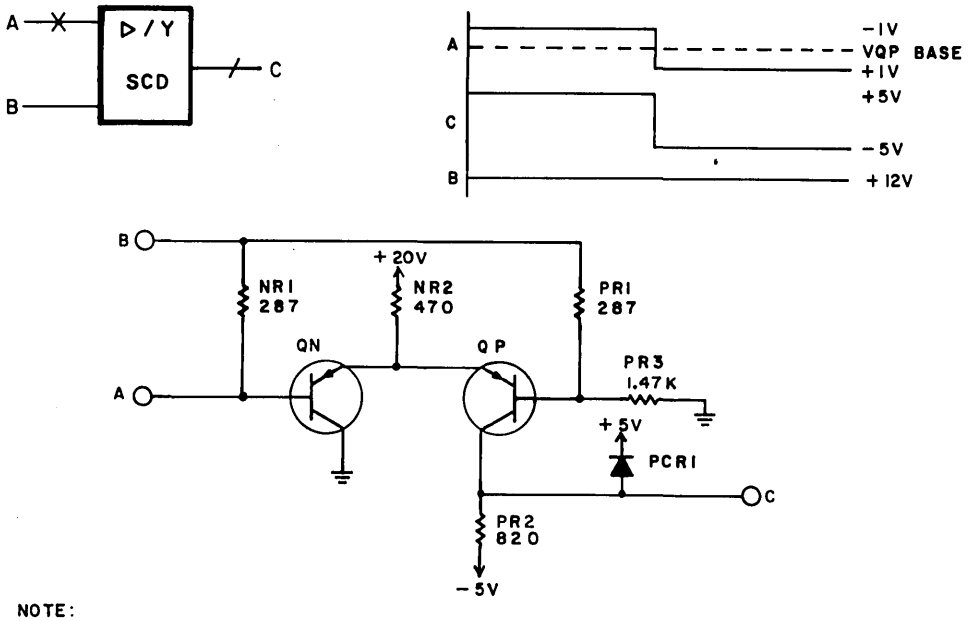
NOTE: VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY.

6T140A

VOLTAGE COMPARATOR - SCD

The SCD circuit compares a voltage at its input (A) against a reference voltage and outputs a bi-level digital signal at C.

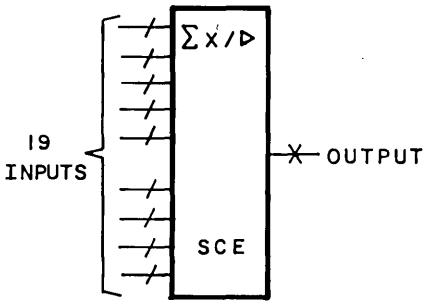
Input A typically is connected to the output of circuit SCE. Input B is typically +12 volts, and normal or "no fault" condition would be for 0 or 1 of the inputs of the summing ladder (SCE) to be grounded and the remaining inputs to be open. SCE would then output a voltage (to input A) higher than the reference voltage at the base of QP. QN then would be turned off and QP turned on driving output C to +5 volts. An abnormal or "fault" condition would be for two or more inputs of the summing ladder (SCE) to be grounded with the remaining inputs open. This would cause the voltage at point A to be lower than the reference voltage at the base of QP. QN would then be turned on and QP turned off. Point C would then switch to -5 volts.

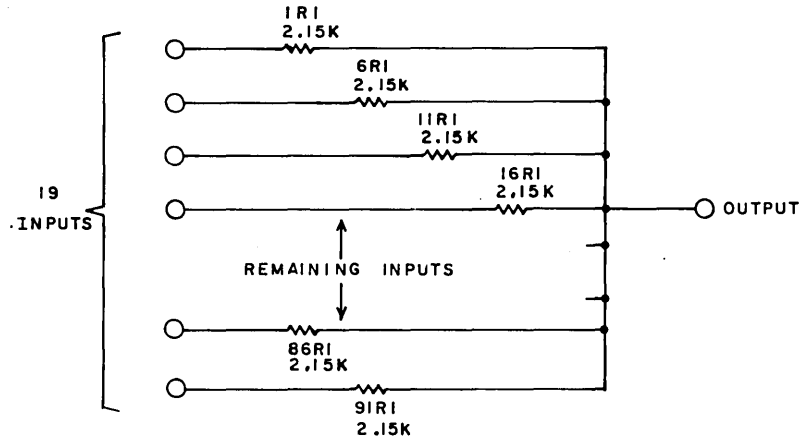


NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J35A

SUMMING LADDER - SCE

The summing ladder SCE circuit is a network of resistors with the output connected to a voltage source through a common resistor such as input A on the SCD circuit. This forms a resistor divider circuit with an output voltage dependent upon the number of inputs (resistors) being connected to ground potential. One or more comparators could be connected to the output to check for a particular number of inputs being connected to ground.





NOTE:
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TFT

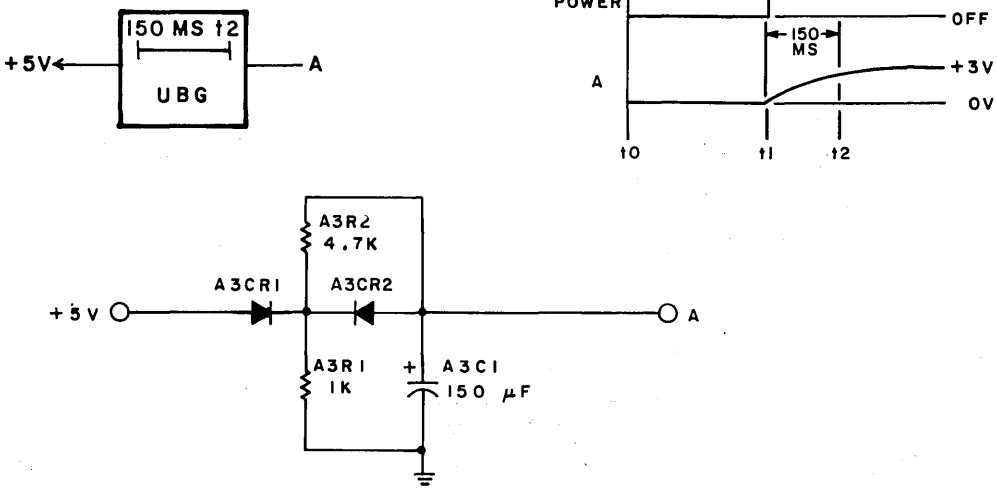
Information not available at time of printing. It will be supplied at a later revision.

DELAY - UBG

The UBG circuit is used to delay application of +5 volts during a power up sequence. Output A drives a standard TTL gate (element number 140).

During a power off phase (t_0), capacitor A3C1 is discharged. When power is applied (t_1), input A is still below the turn-on threshold of the TTL gate due to the discharged state of A3C1. However, the capacitor begins charging through A3CR1, A3R2 and the input resistance of the TTL gate. At time t_2 the capacitor voltage reaches the turn-on threshold of the TTL gate (approximately 1.5v). The capacitor then continues to charge to full capacity.

When the +5 voltage is removed, A3C1 discharges through A3CR2 and A3R1 returning circuit output A to a level below the turn-on threshold of the TTL gate.



NOTE:
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7J37

DELAY - UBD/UBE/UBF/UBH

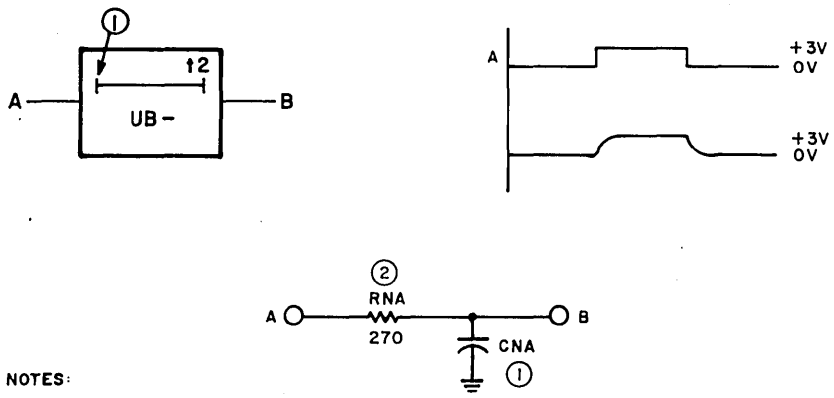
The capacitor delay circuits delay a "1" input at A for a specified period of time before providing a "1" output at B. Delay time for a "0" pulse is negligible.

Assume a "0", ground, enters at A. If the capacitor is discharged, it remains discharged and the output remains "0". If the capacitor is charged when the "0" signal appears, the capacitor discharges almost instantaneously, and the "0" appears with no noticeable delay.

If a "1", +3 volts, enters A while the capacitor is discharged, the capacitor must first charge to a minimum "1" voltage before a "1" can appear at B. The required charge time is the delay time of the circuit. The charge time is dependent on the capacitor value, the resistance between the source voltage and the capacitor, and the minimum voltage required to produce a "1" output.

Delay times for capacitive delays used are as follows:

Delay Type	Time
UBD	200 nsec
UBE	0.5 ms
UBF	0.2 ms
UBH	100 nsec

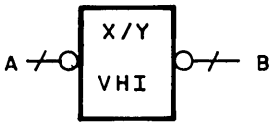


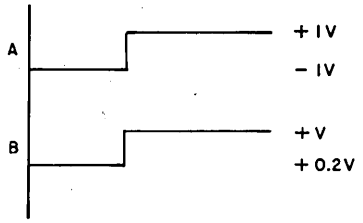
RELAY DRIVER - VHI

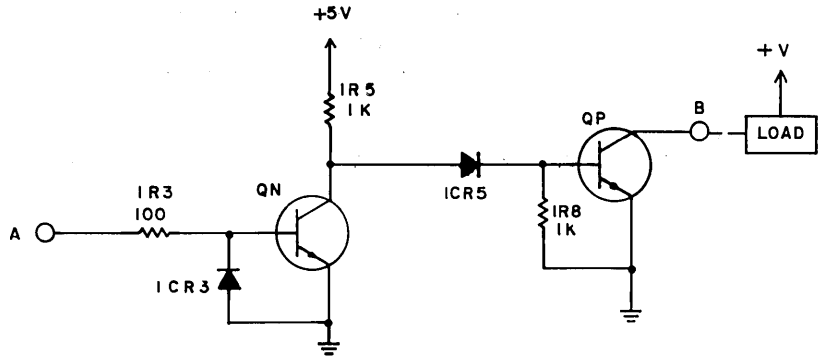
The VHI circuit drives a relay armature terminated at +V volts. Output B of the circuit functions to apply or remove ground so that the +V source may pull or drop the relay.

An input of +1 volt at A turns transistor QN on. The collector of QN goes low which turns transistor QP off. As a result, output B goes to +V and the relay is de-energized.

A -1 volt at input A turns off transistor QN. (Diode CR3 limits the reverse bias on QN to -0.7 volts.) The collector of QN now goes high which turns on transistor QP. This causes output B to go low, near 0 volts, energizing the load.





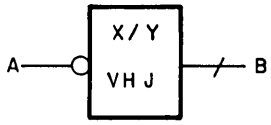


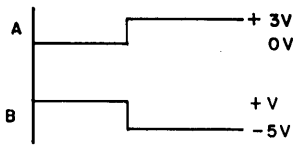
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J38

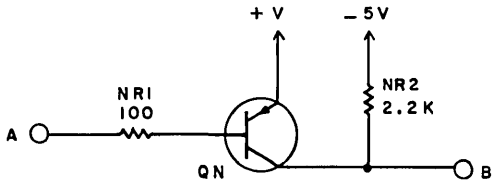
LEVEL TRANSLATOR - VHJ

The VHJ circuit converts TTL logic levels to +V and -5 volt levels where +V = 1.4 to 2.4 volts.

When a "0" (0v to +.4v) is applied to input A, QN turns on and applies +V (minus V_{ce} sat) to output B. When a "1" (+2.4v to +5v) is applied to A, QN turns off and output B switches to -5 volts.







NOTE:
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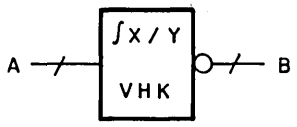
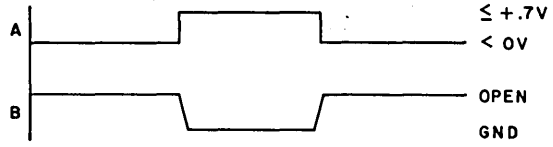
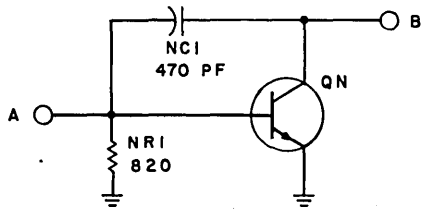
INTEGRATING LEVEL TRANSLATOR - VHK

The VHK circuit is a voltage level shifter that slows down and controls "turn on" and "turn off" transition times.

With an input to A of +.7 volts or greater (current limited to 20 ma), QN turns on with output B going to ground at a rate controlled by collector-base feedback capacitor NC1. With an input of 0 volts to -3 volts, QN turns off and output B is disconnected from ground.







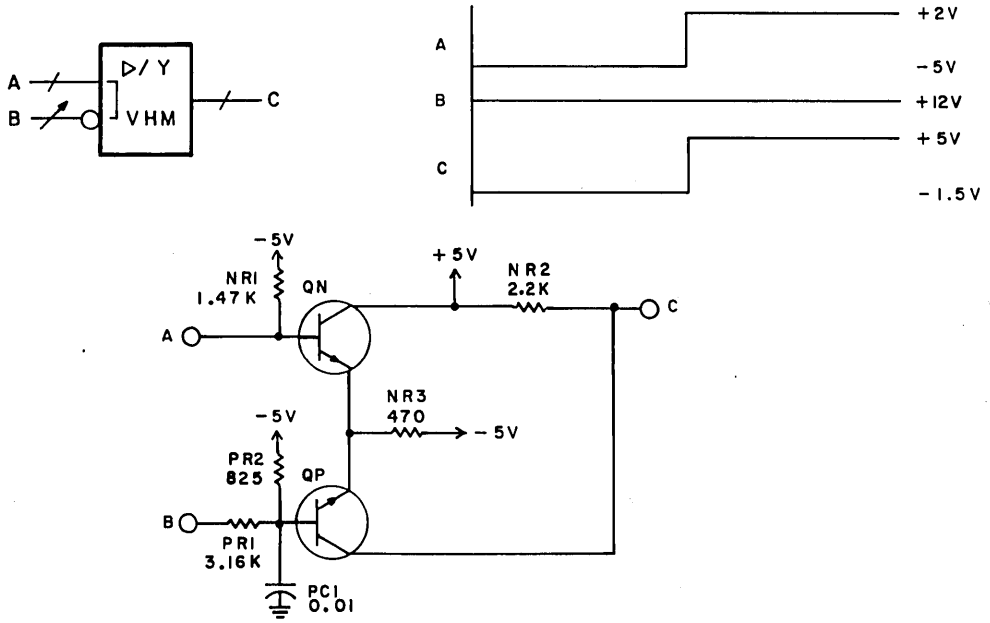
NOTE:
VOLTAGE AND COMPONENT VALUES ARE FOR REFERENCE ONLY. 7J40

FAULT DETECTOR - VHM

The VHM circuit compares a voltage at its input (A) against a reference voltage and outputs a bi-level digital signal at C.

Input A is typically connected to output G of a write driver (JAG) circuit. Input B is connected to a controlled current source (FAG) with an output between +12 to +15 volts, dependent upon the current drain at QP.

The voltage level at input A is determined by the current flow into A through NR1 to -5 volts. With no current into A (A low) the voltage at A is -5 volts which is less than the voltage at the base of QP. QN is off, QP is on, and output C gets clamped at the saturated level of about -1.5 volts or at -.7 volts if output C is connected to a TTL gate input that has a diode clamp. When current flow into A exceeds approximately 2.7 ma, the voltage at A becomes more positive than at the base of QP. QN turns on, QP turns off, and output C rises to +5 volts.



NOTE:
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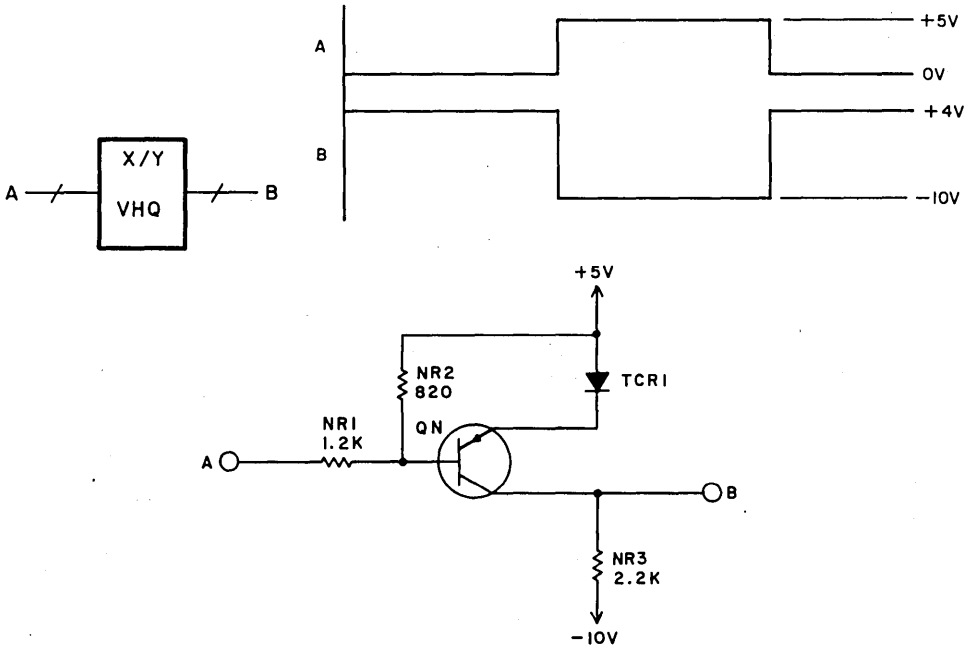
LEVEL TRANSLATOR - VHQ

The VHQ circuit translates digital signal levels of 0v and +5v to digital levels of +4v and -10v respectively.

A "0" (0v to +.5v) at input A causes QN to turn on and apply +5v minus V_{TCR1} or about +4 volts at output B.

A "1" (input open or +5 volts) at input A causes QN to turn off and output B goes to -10 volts through load resistor NR3.

An open collector IC or discrete transistor is used to provide the described input conditions at input A.



NOTE:
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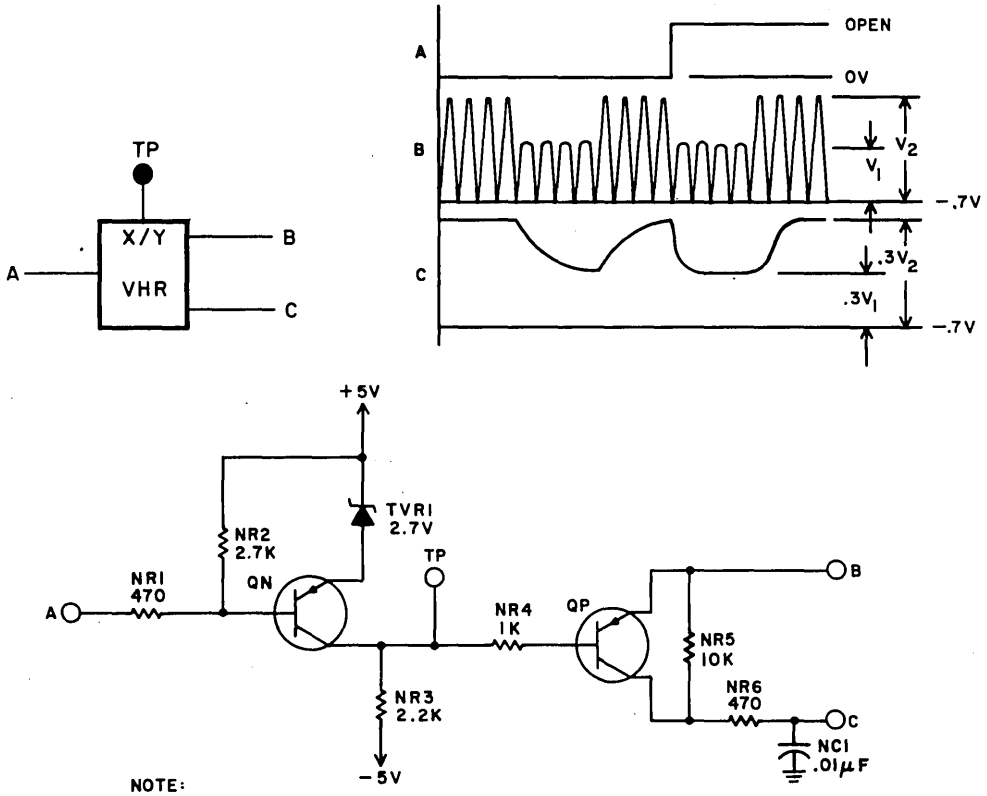
TIME CONSTANT SWITCH - VHR

The VHR circuit converts digital signals to integrator response times by switching a resistor in and out of an RC circuit. The integrator is made up of NR5, NR6, and NC1 with the input at B and output at C. The response time of this integrator can be changed by causing QP to switch NR5 in or out of the circuit.

Full wave rectification of read head signals is entered at B. The integrated output at C is a DC level which is an average value of the input signal waveform.

A "0" (0v to +.5v) at input A causes QN to turn on and apply +5v minus V_{TVR1} or about +2 volts at the base of QP. This causes QP to turn off which inputs NR5 in series with NR6 and the time constant (response time) of the integrator becomes (NR5 + NR6) times (NC1).

A "1" (input open or +5 volts) at input A causes QN to turn off. QN collector goes toward -5 volts through NR3. This causes QP to turn on which "shorts out" NR5 leaving NR6 and NC1 to form the integrator. The time constant (response time) then becomes (NR6) times (NC1).



NOTE:
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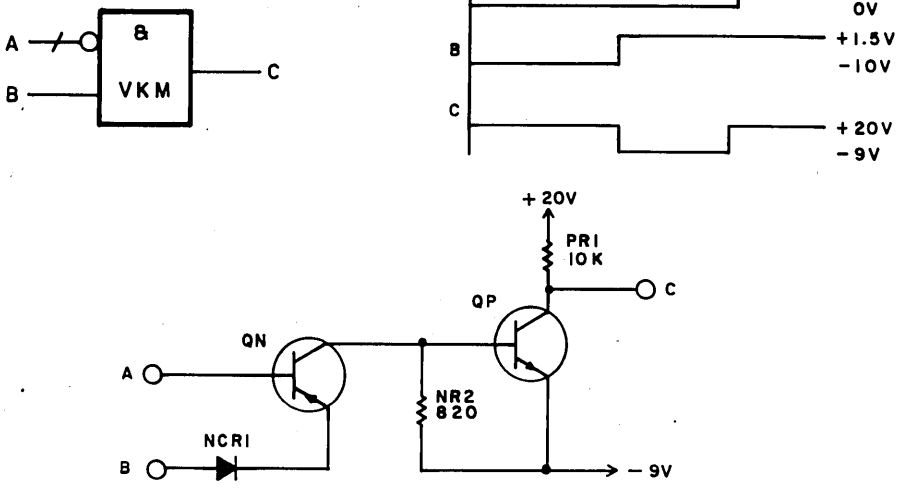
7J99A

AND GATE - VKM

The VKM circuit is a two input gate with output levels of +20 volts and -9 volts.

Input A is typically connected to output B of VHK circuit and input B is connected to output C of VKN circuit through an 820 ohm current limiting resistor.

Diode NCR1 provides breakdown protection for the base emitter junction of QN when inputs A and B conditions cause reverse bias.



NOTE:
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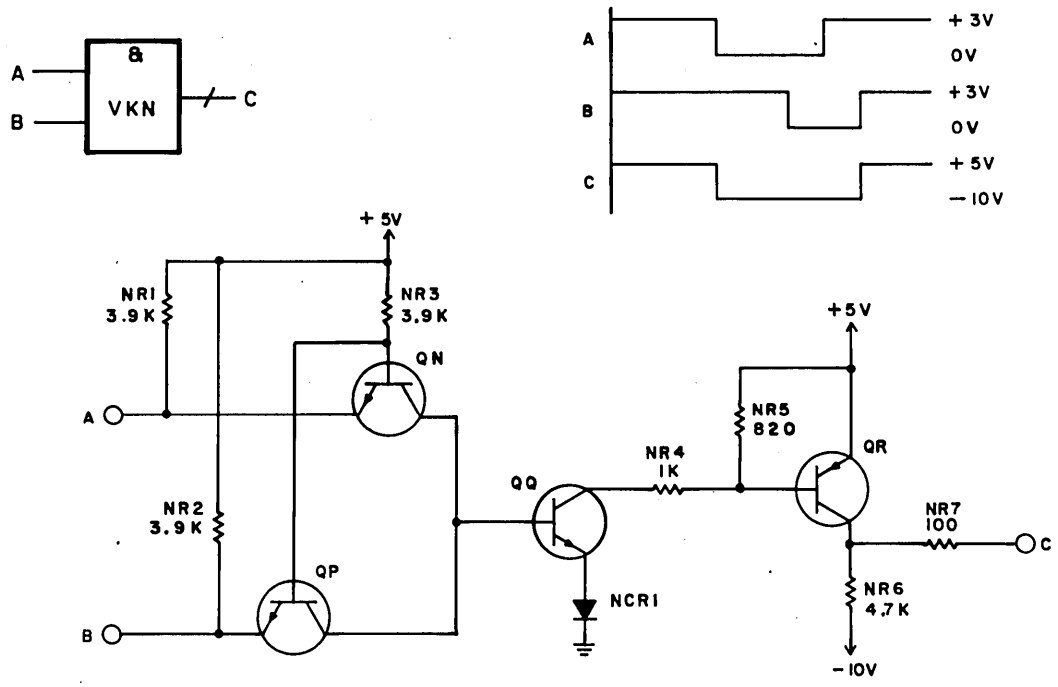
TWO INPUT AND GATE - VKN

The VKN circuit is a two input AND gate with input voltage levels matched to TTL threshold levels (approximately 1.4 volts) by NCR1.

Output voltages of +5 or -10 volts are current limited by resistors NR7 and NR6.



NOTE:
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7J44

DELAY - XAH

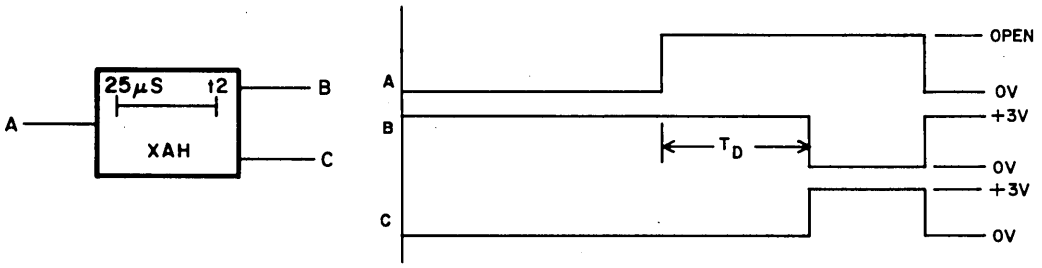
The XAH circuit consists of a one shot integrated circuit (with external RC network) used in an application which results in delayed outputs rather than one shot pulse outputs.

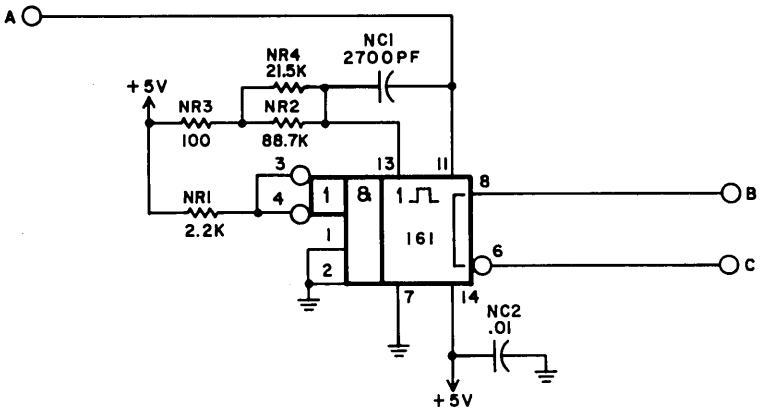
A "0" (0v to +.5v) at input A (pin 11) causes outputs B and C to remain in an inactive state, "1" and "0" respectively.

When input A is released or open, the delay time out begins. At the end of the delay time, outputs B and C change state to a "0" and "1" respectively. The delay time is approximatedby TD=.32 RC, where C=NC1 and R=NR3 + NR2//NR4. A return to a "0" at input A immediately resets outputs B and C to their original states of "1" and "0" respectively.

An open collector output integrated circuit such as a 173H or 200 is used to provide the described input conditions at A.

Resistor RN1 is an input gate pullup to ensure a constant "1" condition on pins 3 and 4.





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